MA1723 HF DRIVE UNIT

TECHNICAL MANUAL

CONTENTS

TECHNICAL SPECIFICATION

Frequency range:	1 to 30 MHz in 100 Hz steps.
Channel storage:	Up to 100 channels of frequency and mode information. Storage time greater than 12 months.
Frequency stability:	(a) Using Racal-Dana type 9442 Ovened Crystal Oscillator. (i) Temperature: ± 6 in $10^{10}/^{o}C$. (ii) Long term: ± 5 in 10^{10} per day after 3 months continuous operation. (b) Provision is made for the use of a Racal-Dana type 9420 standard or an external frequency generating source.
Modes of emission: (see Table 1)	USB/LSB (R3E, J3E) Compatible AM (H3E) ISB (B7E, B8E or B9E) CW (A1A) FSK (F1B)
Carrier suppression:	Suppressed -50 dB Preset internally from -10 dB to -30 dB in 1 dB steps. For remote control the choice of levels is -6, -10, -16, -20 and -26 dB only, in addition to full suppression of better than -50 dB.
Unwanted sideband suppression:	Better than 50 dB relative to PEP.
Power output:	200 mW maximum into 50 ohm load, adjustable by internal preset. The set power level will not deviate by more than ± 1 dB over the full frequency range with a change of $\pm 10^{o}C$ from ambient temperature.
Audio input level:	-30 dBm to +10 dBm into 600 ohm (balanced) by preset adjustment.
Audio AGC:	An audio input variation of ± 10 dBm relative to an input signal between -20 dBm and 0 dBm will produce a change in output level of less than 2 dB.
Intermodulation Products:	Better than -50 dB relative to either one of two equal tones in a standard two tone test.
Hum:	Bettery than -50 dB relative to PEP.
Spurious emissions excluding harmonics:	Better than -55 dB relative to PEP.

Wideband noise:	Better than -110 dB relative to PEP in a 3.0 kHz bandwidth 500 kHz off tune.
Muting level:	Better than 70 dB below PEP.
RTTY keying input:	Neutral or polar keying, +5 V, -5 V or -5 V:0:+5 V from external source. Input impedance 500 ohm. Sense reversal by internal link.
Frequency shift:	85 Hz to 850 Hz by preset adjustment. Centre frequency - nominal carrier (FSK) or 2 kHz offset from nominal carrier (ISB2, ISB3). Stability within 2% of total deviation.
On/Off keying ratio:	Better than 55 dB.
Environmental:	Designed to operate to full specification under the following temperature conditions:
	(a) Operating -10°C to +55°C
	(b) Storage -40°C to +70°C
	(c) Relative Humidity 95% at 40°C
Dimensions:	Height: 133 mm (5.25 in)
	Width: 483 mm (19.0 in)
	Depth: 450 mm (17.7 in)
Weight:	Approximately 20 kg (44 lb)
Power supply:	100, 120, 220, 240 V taps, +10% to -15% on nominal tap voltage 45-65 Hz.

ACCESSORIES

AA650/H	Fist microphone, carbon insert, with pressel switch and coiled lead terminated in PO plug 420.
AA651/G	Handset, carbon microphone, EM receiver (300 ohm), with pressel switch and coiled lead terminated in PO plug 420. Supplied with AA652/B stowage bracket.
AA653/J	Desk microphone, carbon insert, with pressel switch and lead terminated in PO plug 420.
AA655/L	Boom micrphone and headset, carbon microphone, EM receiver, pressel switch with lapel clip, and lead terminated in PO plug 420.
AA670/B	Morse key, silver contacts, with unterminated lead.
AA671/E	Miniature morse key with knee strap and unterminated lead.

Classification and Designation of Emissions

The symbols given in brackets against Modes of Emission conform to CCIR Recommendation 507, published by the International Telecommunication Union (ITU), Volume 1, 1978. CCIR Recommendation 507 replaces a former ITU document, Radio Regulations Article 2 (RR2), and Table 1 provides a comparison, where possible, of the two documents for the modes of emission applicable to the MA 1723.

Table 1: Modes of Emission

MODE	CCIR 507	ITU RR2
USB/LSB	R3E	A3A
	J3E	A3J
ISB	B7E	-
	B8E	A3B
	B9E	-
CW	A1A	A1
FSK	F1B	F1

CHAPTER 1

GENERAL DESCRIPTION

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CHAPTER 1

GENERAL DESCRIPTION

INTRODUCTION

1. The MA 1723 is a synthesized HF transmitter drive unit covering the frequency range 1 MHz to 30 MHz in 100 Hz increments. The operating modes include USB, LSB, ISB with either suppressed or pilot carrier, compatible AM (A3H), CW (true keyed carrier) and FSK (optional). The pilot carrier level can be preset in 1 dB steps over the range -10 dB to -30 dB. The RF output level may be preset to any level between 25 mW and 200 mW by the adjustment of an internal control.

BRIEF TECHNICAL DESCRIPTION

2. For explanation purposes, the drive unit is divided into two sections, namely the AF/IF/RF section, and the control and display section. These sections are described in the following paragraphs in conjunction with the block diagrams given in figs. 1.1 and 1.2 at the end of the chapter.

AF/IF/RF Section (Fig. 1.1)

3. This section embraces the modulation board, the mixer board and the RF output board, together with the optional FSK board and parts of the front panel display board, the front panel interface board, and the rear panel board. The balanced line 1 and/or line 2 audio inputs applied to the rear panel are routed to the modulation board via isolation transformers and preset level controls, whilst the output from a carbon microphone connected to the LINE 1 or LINE 2 socket on the front panel is routed to the modulation board via an amplifier stage on the front panel display board. C-MOS analogue switches are used to route the incoming audio signal to either the USB or LSB balanced modulator and crystal fitter. A level control circuit reduces the sideband level by 6 dB in the ISB and AM modes (to maintain the correct peak envelope power) and is also used to mute the sideband when it is not selected.

4. The balanced modulators consist of diode ring mixers which combine the audio signal with a 1.4 MHz carrier to produce a double-sideband suppressed-carrier signal. The wanted sideband is then selected using a 1.4 MHz crystal fitter, and the two sidebands are combined with the reinserted 1.4 MHz carrier in a summing amplifier. The gain of this amplifier is reduced by a preset amount when LOW POWER is selected at the front panel.

5. For CW operation the key input is fed via a shaping circuit to a carrier level control circuit for ON-OFF keying of the carrier. The shaping circuit produces a keyed signal which complies with CCIR recommendation 328-4 at a keying rate of 25 words per minute (20 bauds).

6. The carrier levels required for the 'pilot carrier' and 'tune' modes can be preset and stored in memory by the operator, for automatic recall when the particular mode is selected.

7. The 1.4 MHz output signal from the modulation board is applied to the mixer board where it is mixed with a 40 MHz signal from the control and display section. A band pass filter selects the sum frequency output, and this is applied to a further mixer where it is mixed with a 42.4 MHz to 71.4 MHz local oscillator signal to produce an output signal in the range 1 MHz to 30 MHz. The final mixer output signal is filtered using a 30 MHz low pass filter, and is then amplified before application to the RF output amplifier board. This contains a three-stage transformer-coupled broad-band amplifier which produces an output in the range 25 mW to 200 mW, adjustable by a preset resistor.

8. The optional FSK board contains an audio oscillator which is shifted between two frequencies to produce a tone shift keyed (TSK) signal centred on 2 kHz. This is then transmitted as an upper sideband suppressed carrier signal and the 42.4 MHz to 71.4 MHz local oscillator signal is shifted by 2 kHz so that the transmitted signal is centred on the selected operating frequency, as displayed on the front panel. The frequency shift is adjustable in the range plus and minus 42 Hz to plus and minus 425 Hz, using an internal preset control. The frequency shift keying is shaped to meet the bandwidth requirements of CCIR recommendation 328-4 at a keying rate of 200 bauds.

9. In addition to the normal FSK mode, two ISB modes are provided where audio from a line input is transmitted in one sideband, and a TSK signal centred on 2 kHz is transmitted in the other sideband.

Control and Display Section (fig. 1.2)

10. This section comprises the reference generator board, the synthesizer board, the front panel display board, the front panel interface board, the processor board and the optional remote interface board. The control is based on a microcomputer assembly (located on the processor board) which comprises an 8-bit C-MOS central processing unit (CPU), 12 k bytes of read only memory (ROM), in which is stored the operating program and a number of test programs, 256 bytes of random access memory (RAM), 1 k byte of electrically alterable read only memory (EAROM) and a programmable input/output device. The 256 byte RAM is used by the CPU for temporary data storage, whilst the EAROM is used for the storage of pre-programmed channel information (channels 00 to 99), as well as the storage of the current drive unit control settings so that the unit returns to these same settings following an interruption in the supply.

11. The PIO device has two high-speed 8-bit I/O ports. One of these is used as a bi-directional data bus for the transfer of data between the CPU and other parts of the unit, whilst the other is primarily used for the generation of a number of strobe pulses.

12. The front panel display board contains the keyboard and the displays. The keyboard (i.e. the 28 front-panel pushbuttons) are connected as a four-column by eight row matrix which is continually strobed by the processor via circuitry on the front panel interface board. This latter board also contains a 16-line multiplexer which is used in conjunction with a digital-to-analogue converter and a voltage comparator to monitor a variety of analogue signals, such as the carrier level, and the regulated voltage supplies.

13. The reference generator board accepts the output from the optional internal 5 MHz frequency standard or the output from an external frequency standard (which may be any sub-multiple of 20 MHz from 10 MHz down to and including 100 kHz). When an external frequency standard is connected to the drive unit, it automatically overrides the internal frequency standard (if fitted). A 20 MHz reference signal, which is prooduce using a voltage controlled oscillator (VCO) within a phase-locked loop, is applied to the synthesizer board, and is also used to prduce outputs at 1.4 MHz and 40 MHz for application to the modulation and mixer boards respectively.

14. The synthesizer board contains the 42.4 MHz to 71.4 MHz local oscillator single-loop synthesizer circuit. An output signal from the VCO is applied to a programmable divide-by-N stage, where the value of N is determined by the most significant digits of the required output frequency. The least significant digits of the required output frequency (those below the sampling frequency of 1 MHz) are used to compute a phase offset control voltage which is fed into the loop (via a digital-to-analogue converter) as an extra input. The loop adjusts the VCO phase to be the sum of the reference phase (i.e. that resulting from the comparison between the 1 MHz reference and the output signal from the divide-by-N stage) and the computed phase.

15. One type of optional remote interface board available is the SCORE interface board (SCORE stands for Serial Control of Racal Equipment). This allows for extended control (hard wired) or full remote control (data modems), using a control unit such as the Racal MA 1090. The SCORE system is based on a number of 48-bit synchronous frames, each of which contain a 16-bit preamble (synchronisation, word number identification, etc.) followed by a 32-bit data word. Separate lines are used for both data and clock signals travelling in each direction. These comply with CCITT V10 and are thus compatible with a wide variety of data modems.

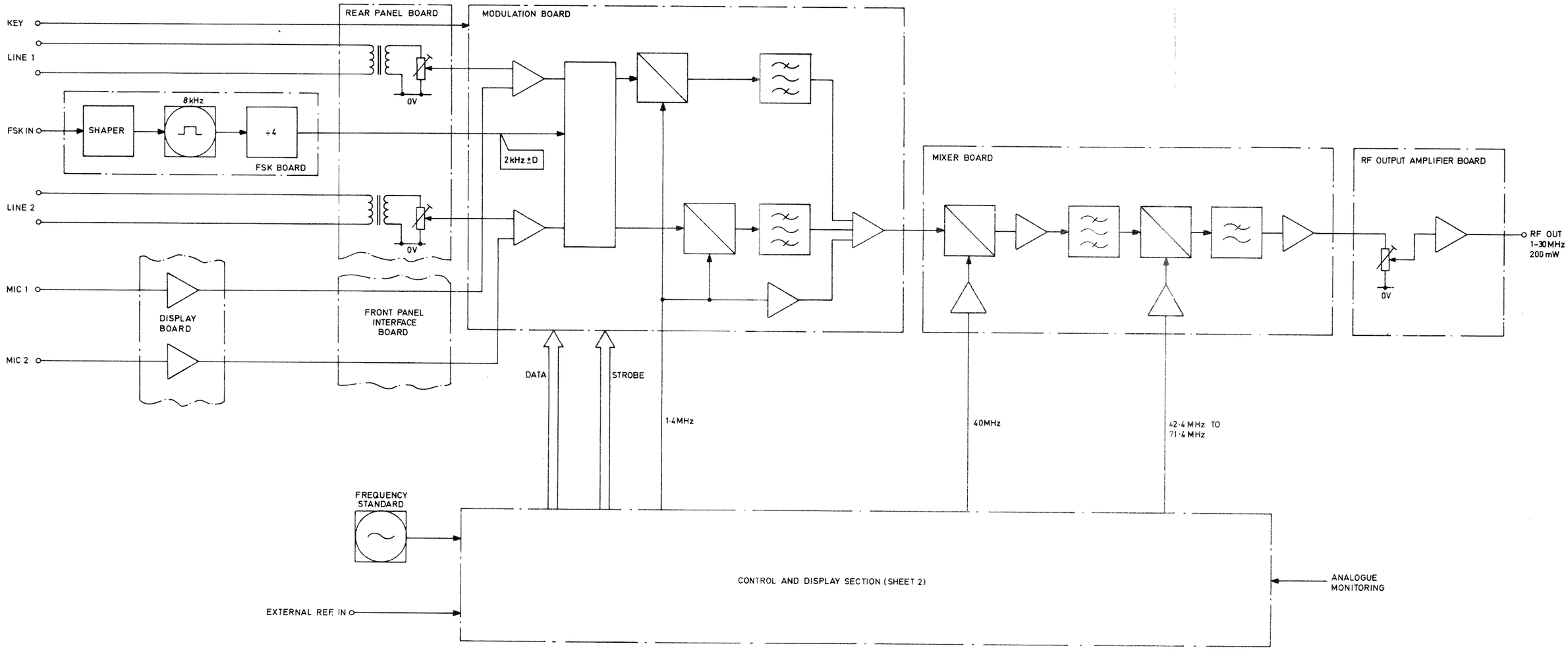
PHYSICAL DESCRIPTION (figs. 1.3 and 1.4)

16. A full-width, compartmented, cast-aluminium chassis forms the basis of the drive unit. The synthesizer, reference generator and mixer boards are housed in the screened compartments in the underside of the cast chassis; these compartments are provided with push-fit metal covers to adequately screen each board. On the top of the chassis are mounted the modulation board, RF output board, optional frequency standard, optional remote interface board and the power supply module. The optional FSK board is mounted either in place of the remote interface board or on pillars above it. The processor board is mounted on the inner face of the right-hand side member whilst the audio and control connectors are mounted on the rear panel board. The removable front panel assembly consists of the front panel and a front sub-panel to which are mounted the front panel display board and the front panel interface board. Plan and underside views of the unit are given in figs. 1.3 and 1.4 at the end of the chapter.

IDENTIFICATION OF VARIANTS

17. In order to identify the optional facilities fitted to a particular drive unit, an option label is attached to the rear panel. The meanings of the option label codes are as follows:

First character:	Identification of 1.4 MHz sideband filters fitted. B3 - standard 3 kHz filters B6 - standard 6 kHz filters.
Second character:	Frequency Standard. O indicates no internal frequency standard fitted. Unit operates from an external standard. S2 indicates type 9442 fitted. S3 indicates type 9420 fitted.
Third character:	Remote Interface. O indicates no remote interface board fitted. S denotes SCORE interface board fitted. C indicates Channel interface board fitted.
Fourth character:	FSK Board. O indicates not fitted. F indicates is fitted.



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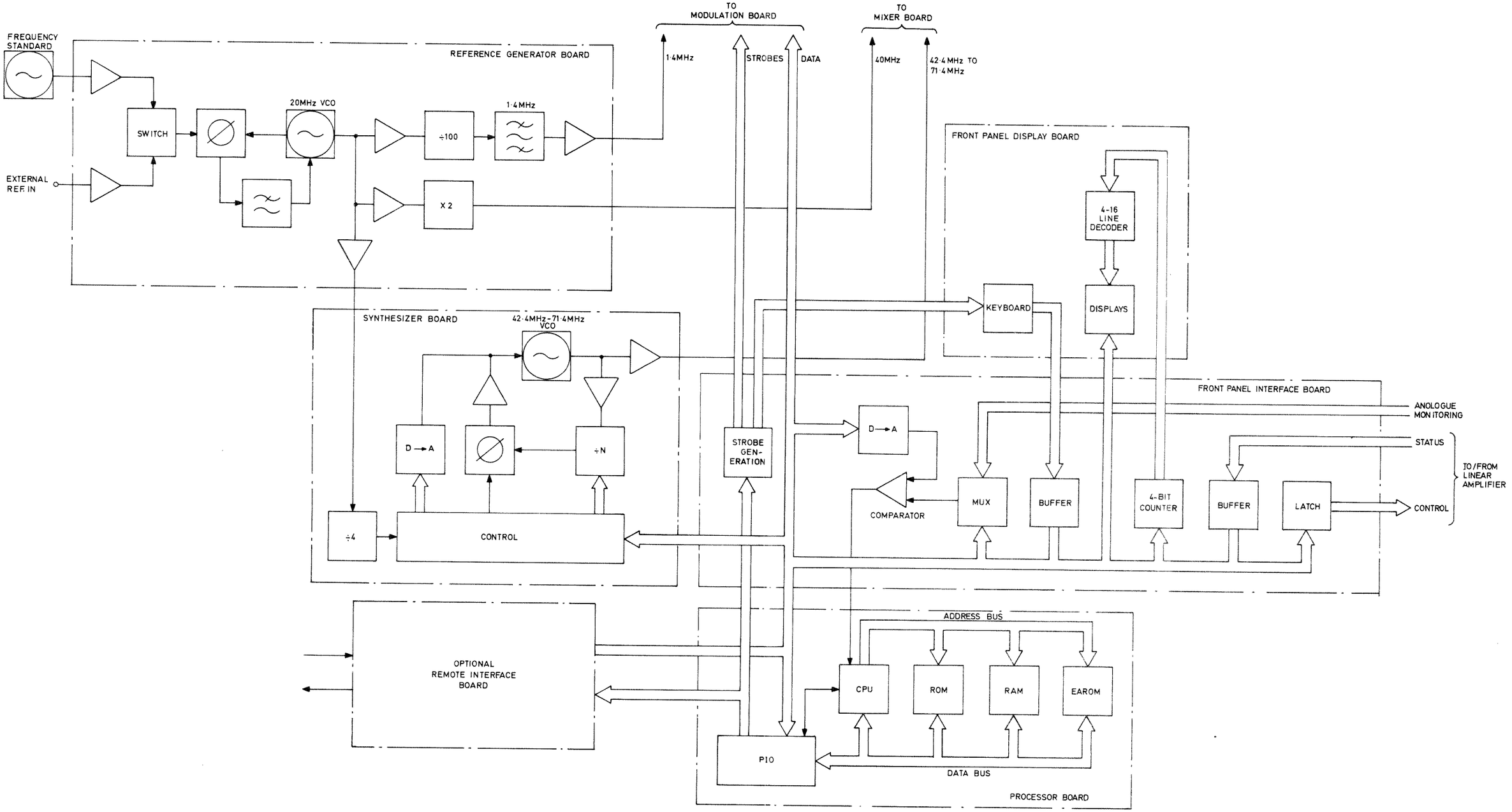
Block Diagram: MA1723 (Sheet 1)

Fig. 1.1



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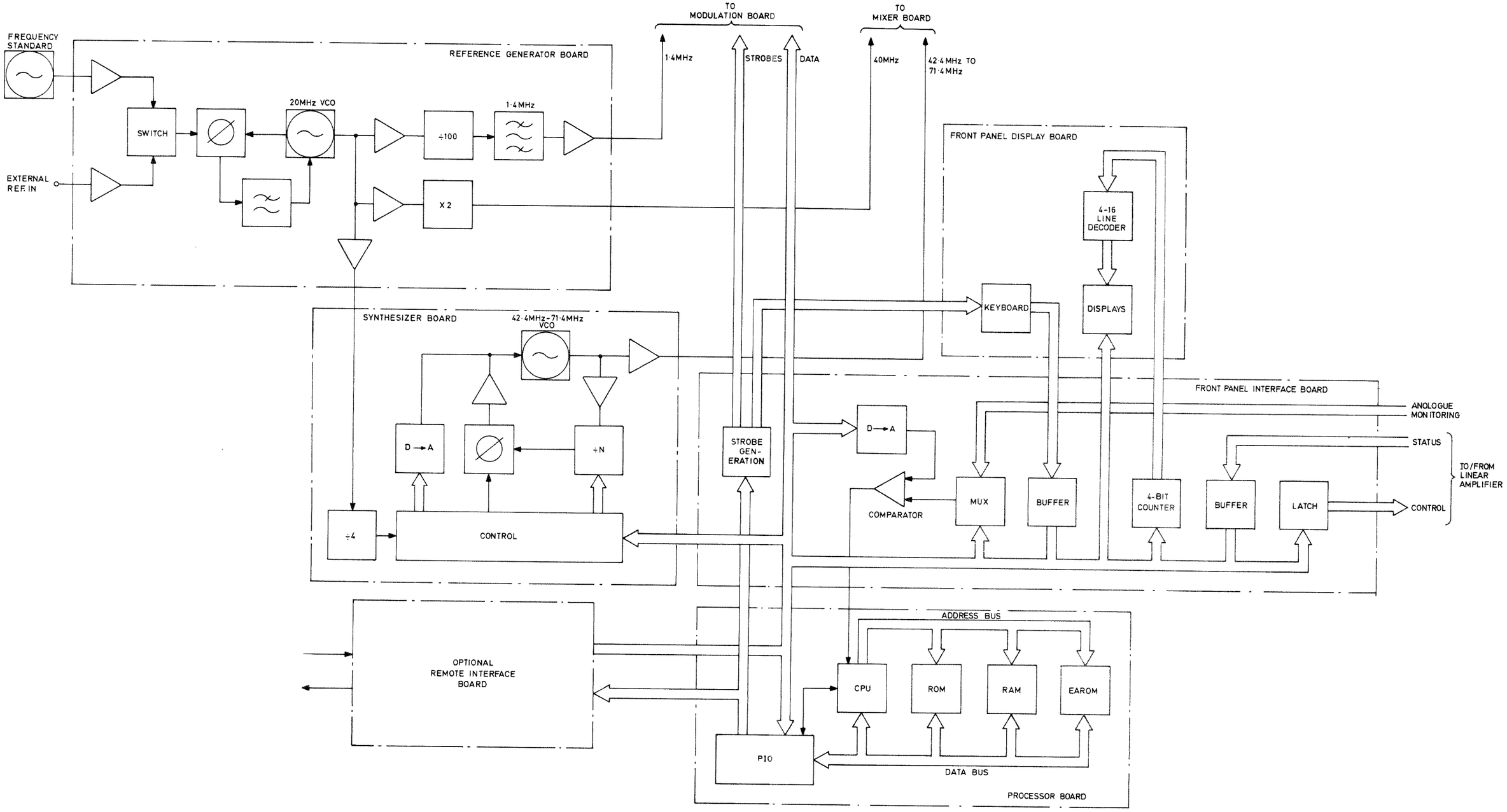
Block Diagram: MA1723
(Sheet 2)

Fig. 1.2



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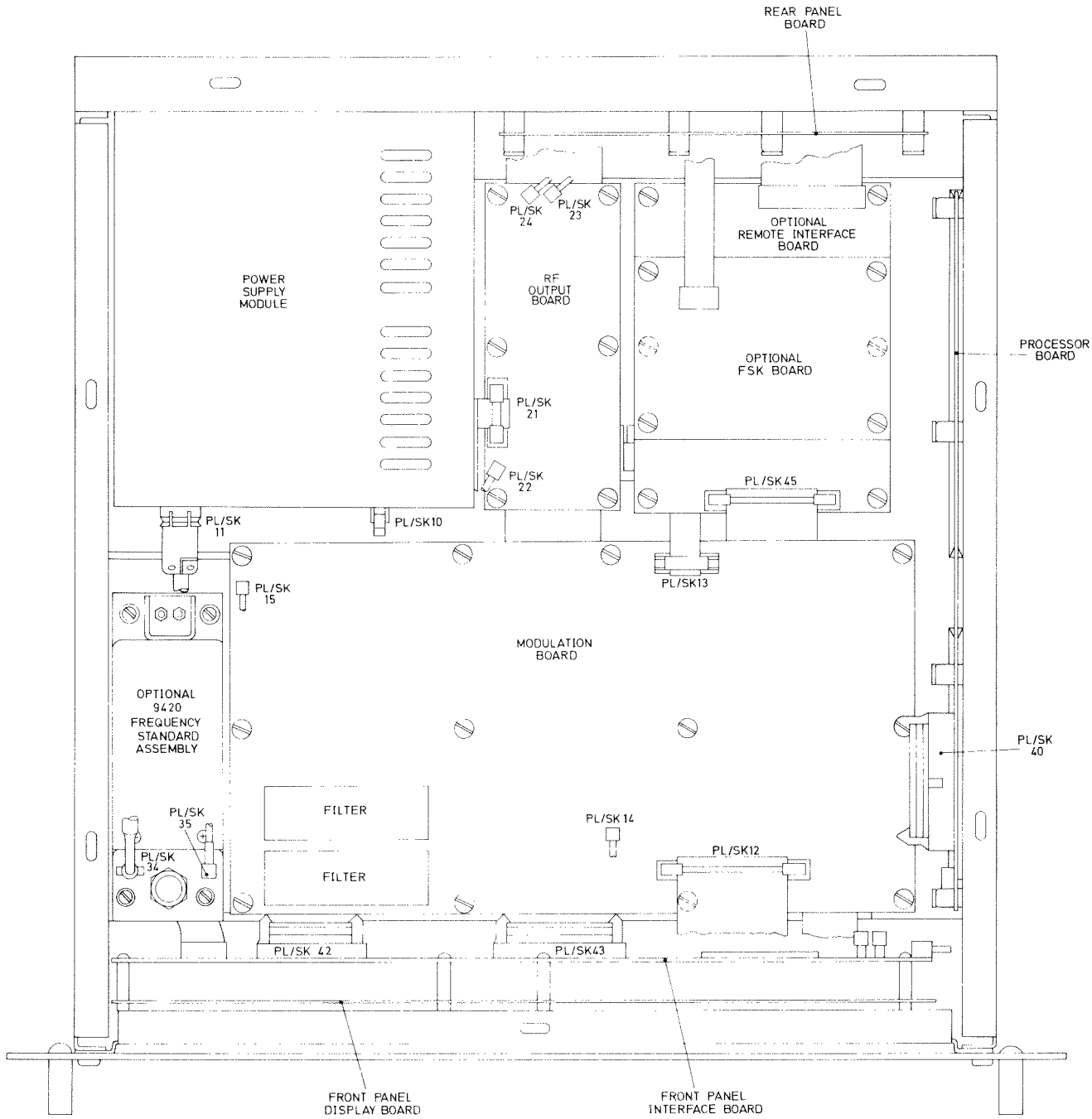
Block Diagram: MA1723 (Sheet 2)

Fig. 1.2



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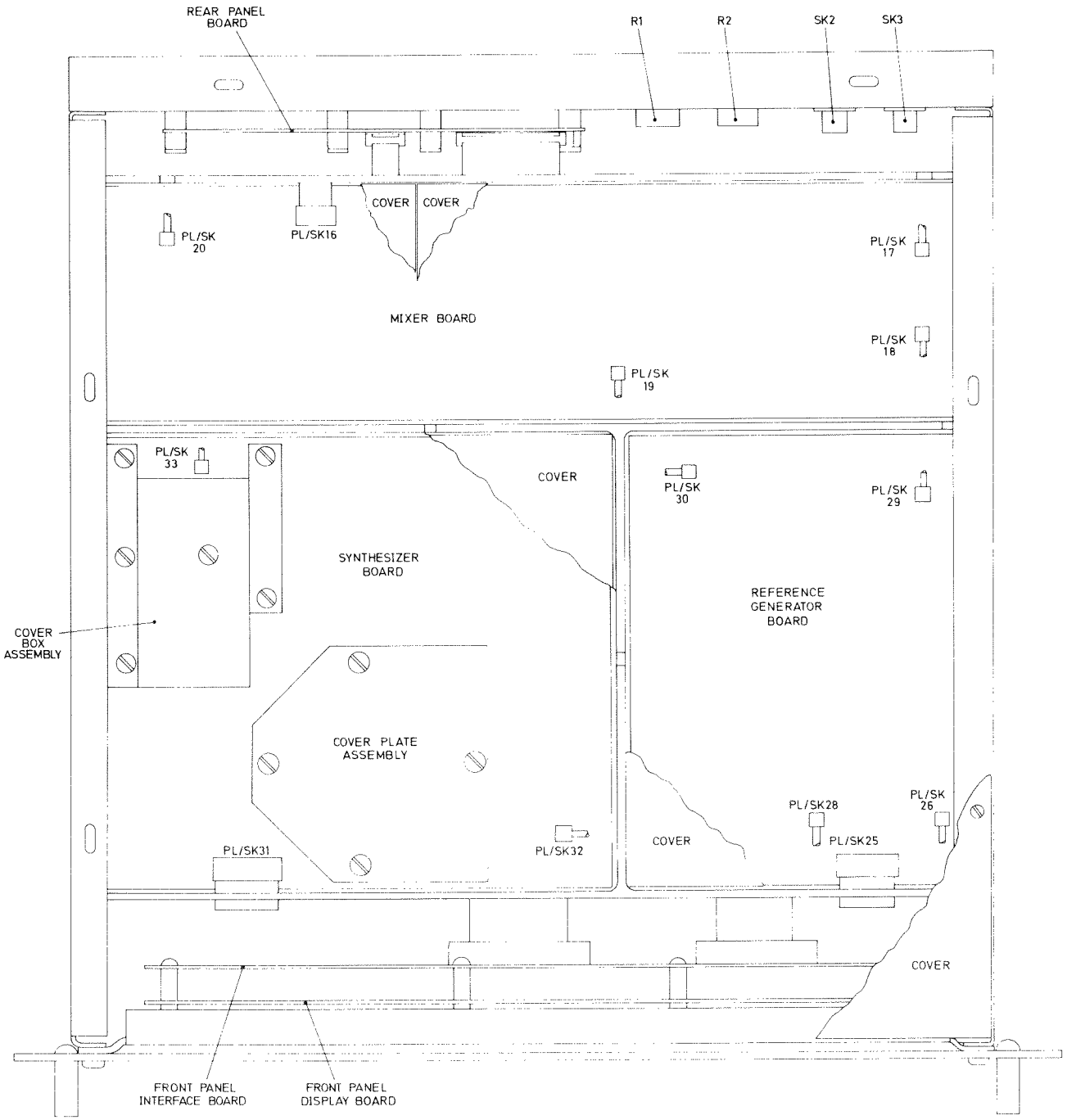
Plan View : MA1723

Fig. 1.3



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Underside View : MA1723

Fig. 1-4

CHAPTER 2

INSTALLATION

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CHAPTER 2

INSTALLATION

INTRODUCTION

1. This chapter provides general installation information only. For information concerning specific installations, reference should be made to the appropriate system manuals.

REAR PANEL CONNECTIONS

2. A brief description of each rear panel connection is given. Refer to fig. 2.1 at the end of the chapter for a rear panel view of the unit.

Power Input Connector

3. The power supply input connection mates with PL1 using a 3-way socket (Racal part number 930766). The connections are as follows:

L	LIVE
N	NEUTRAL
⏚	EARTH

CAUTION Ensure that the voltage selector is correctly set before connecting the unit to the source of supply (para. 6).

Power Fuse

4. The fuse fitted to the drive unit should be a slow blow type, rated at 1 A (Racal 934804). A further fuse, rated at 2 A (Racal 922449), is mounted on the power supply module chassis, and is only accessible after the removal of the overall top cover plate from the unit. This fuse (FS2) protects unregulated supply lines designated + 5 V UNREG A and B.

5. The power fuse is located in a compartment adjacent to the supply connector. To gain access, remove the mating power input socket and slide the transparent cover to the left to reveal the fuse. To remove the fuse, pull (to the left) the small lever marked FUSE PULL.

Voltage Selector

6. The voltage selector is located beneath the power fuse (para. 5) and consists of a small printed circuit card which may be inserted in one of four different ways (to select 100 V, 120 V, 220 V or 240 V). A small hole is provided in the card to facilitate removal. Ensure that when the card is inserted, the desired voltage setting is visible on the card.

RF Output Connector

7. The RF output connector SK2 is for the connection of a 50 ohm unbalanced coaxial line using a BNC type connector (Racal 900038). The level of RF output may be preset in the range 25 mW to 200 mW (para. 18) to suit the associated amplifier.

External Reference Connector

8. The reference signal requirement of the unit is met using either an internal 5 MHz frequency standard or by the connection of an external standard connected to the REF IN socket SK3 (mating BNC plug Racal 900038). Note that the connection of an external standard (which may be any sub-harmonic of 20 MHz between 100 kHz and 10 MHz) automatically overrides the output from the internal frequency standard (if fitted).

Audio Connector

9. The audio connections (listed in table 1) are made using a 25-way plug which mates with SK4. The Racal part numbers for the mating 25-way plug are as follows:

Plug, 25-way	916489	
Shell, junction, straight		918108
Retainer	914245	

Amplifier Connector

10. The connections between the drive unit and the associated linear amplifier are made using SK6. The connections are as given in table 2; those actually used are dependent upon the particular installation. The Racal part numbers for the mating 15-way plug are as follows:

Plug, 15-way	909729	
Shell, junction, straight		912683
Retainer	914244	

Table 1: Audio Connector SK4

PIN	SIGNAL DESCRIPTION
1	Balanced line 1
2	Audio Input, 600 ohms
14	Line 1 screen
3	Balanced Line 2
4	Audio Input, 600 ohms
16	Line 2 screen
6	Receive Audio 1 in
19	Receive Audio 2 in
18	Receive Audio screen
23	0 V
24	+15 V Out (200 mA maximum)
7	External Mute (0 V = Mute)
12	External PTT (0 V = Transmit)
13	FSK Input
25	FSK Input screen
5	Key Input
17	Key Input screen
20	0 V
8	Matrix Interlock (0 V = Normal)
9	NC
15	Transmit (0 V = Transmit)
22	Power Select A
10	Power Select B
21	Not Used
11	Not Used

Table 2: Amplifier Connector SK6

	PIN	SIGNAL DESCRIPTION
LINEAR AMPLIFIER STATUS LINES	2	FAULT (0 V = FAULT, O/C OR +12 V = Normal)
	3	READY (0 V = READY, O/C OR +12 V = Not Ready)
	10	EHT ON (0 V = ON, O/C OR +12 V = OFF)
	12	STANDBY
	5	REDUCED POWER (0 V = Normal, O/C OR +12 V = Reduced Power)
	14	SPARE
	15	0 V
LINEAR AMPLIFIER CONTROL LINES	1	POWER ON (+12 V = ON, 0 V = OFF)
	6	EHT ON (0 V = ON, O/C = OFF)
	7	STANDBY ON (0 V = ON, O/C = OFF)
	4	RESET (0 V = Normal, O/C = RESET)
	8	MUTE (0 V = MUTE, O/C = Normal)
	11	COARSE TUNE INITIATE (Same as RESET)
	9	0 V
	13	NC

Remote Control Connector

11. This connector (SK5) need by considered only when the unit is fitted with a remote control interface option (such as the SCORE interface board - Chapter 14), and when remote control is required. Table 3 lists the connections applicable when a SCORE interface board is fitted. Connection details for other types of interface board are given in the relevant appendix to this manual or in the appropriate system manual. The Racal part numbers for the mating 37-way plug are as follows:

Plug, 37-way	916507
Shell, junction, straight	918105
Retainer	914246

Table 3: SCORE Interface Connector SK5

PIN	SIGNAL DESCRIPTION
1	0 V
22	W ┐
21	X │ USER FUNCTIONS
2	Y │ OUT
3	Z ┘
4	A ┐
5	B │ USER FUNCTIONS
6	C │ IN
7	D ┘
8	0 V
9	CONTROL DATA IN
10	0 V
11	CONTROL CLOCK IN
12	0 V
13	REVERTIVE DATA OUT
14	0 V
15	REVERTIVE CLOCK OUT
16	0 V
18	0 V
19	0 V
20	0 V
23	0 V
34	0 V
36	0 V
17	┐
24 to 33	│ NO
35	│ CONNECTION
37	┘

Earth Terminal

12. A terminal is provided on the rear panel for connection to the earthing (ground) system of the rack or cabinet.

FRONT PANEL CONNECTIONS

Line Jacks

13. Two audio sockets, designated LINE 1 and LINE 2, are provided on the front panel for the connection of items such as a carbon microphone, telephone handset, boom microphone and headset, etc. Connection is via a standard three-ring and tip Post Office type 420 plug (Racal 933837), conections as follows:

Tip:	PTT
Ring 1 (nearest tip):	Carbon Microphone
Ring 2:	Line Monitor/Sidetone
Ring 3:	Earth

14. For SSB operation, LINE 1 is used for USB or LSB, as selected, and LINE 2 is open circuit. For ISB operation, LINE 1 is used for USB, LINE 2 for LSB.

RF BNC Connector

15. This coaxial socket (mating BNC plug Racal 900038) is for RF output monitoring purposes only.

INTERNAL CONTROLS

Board-mounted Switches

16. Two AGC ON/OFF switches are fitted to the modulation board (the large board mounted on top of the chassis), and six switches are fitted to the processor board (mounted on the right-hand side member). The position of these switches should be checked prior to the installation of the unit into the rack or cabinet, as follows:

(1) Place the unit on a flat, clean working surface.

(2) Remove the overall top cover plate (if fitted), secured with quarter-turn quick-release fasteners.

(3) Locate the six switches on the processor board (SA to SF) and check that all set to the open (OFF) position.

(4) Locate switches SA and SB on the modulation board. Set to the closed (normal) position for AGC ON (SA for USB, SB for LSB), to the open position for AGC OFF.

Line Level Adjustment

17. The two line level potentiometers are mounted on the rear panel (marked LINE 1 and LINE 2), and may be adjusted before the unit is installed into the rack or cabinet, as follows:

(1) Check that the voltage selector is correctly set to suit the intended source of supply (para. 6).

(2) Connect an audio signal generator, set to a frequency of approximately 1 kHz and an output level approximately equal to the intended audio line level, to pins 1 and 2 of SK4 on the rear panel (balanced line 1 audio input, 600 ohms).

(3) Connect a suitable 50 ohm load to the RF OUT socket SK2 on the rear panel. On AMPLIFIER socket SK6 link pin 3 to pin 9.

(4) Connect the unit to the source of supply and set the POWER switch to ON.

(5) Check that REMOTE is not illuminated on the left-hand display panel. If it is, press and release the REM pushbutton.

(6) Press and release the RESET button. Ensure that the associated LED is extinguished and READY is indicated on the right hand display panel.

(7) Press and release either the USB or LSB mode pushbutton and check that the appropriate mode is displayed.

(8) Place the LINE/SET/RF switch to the SET position.

(9) Set the VOX/PTT/TX switch to PTT.

(10) Adjust the LINE 1 control on the rear panel for a front panel AF meter indication of 0 dBm.

(11) Transfer the audio signal generator to pins 3 and 4 of SK4 on the rear panel.

(12) Press and release the ISB1 pushbutton.

(13) Press and release the METER pushbutton so that SET 2 is illuminated on the right-hand display panel.

(14) Adjust the LINE 2 control on the rear panel for a front panel AF meter indication of 0 dBm.

(15) Switch off and disconnect the signal generator.

RF Output Level Adjustment

18. The RF output level may be adjusted over the range 25 mW to 200 mW (+14 dBm to +23 dBm) by the adjustment of R1 on the RF output board (Chapter 1, fig. 1.3), as follows:

(1) Connect a suitable 50 ohm load to the RF OUT socket SK2 on the rear panel. OIn the AMPLIFIER socket SK6 link pin 3 to pin 9. On the AUDIO socket SK4 link pin 5 to 17.

(2) Connect the unit to the source of supply and set the POWER switch to ON.

(3) Check that REMOTE is not illuminated on the left-hand display panel. If it is, press and release the REM pushbutton.

(4) Check that none of the six red status indicators are illuminated. Any that are may be extinguished by pressing and releasing the associated pushbutton. Press and release the RESET button and ensure that the associated LED is extinguished and READY is indicated on the right hand display panel.

(5) Press and release the CW button and ensure that CW is displayed.

(6) Place the LINE/SET/RF switch to the RF position.

(7) Place the VOX/PTT/TX switch to the TX position. Check that TRANSMIT is illuminated on the right-hand display panel.

(8) Adjust R1 on the RF Output board for the required output level, as indicated on the front panel meter (table 4).

Table 4: mW to dBm Conversion

mW	dBm
25	+14
50	+17
80	+19
100	+20
125	+21
160	+22
200	+23

FSK BOARD

19. Links are fitted to the optional FSK board (para. 20) to cater for various types of teleprinter, and the values of two resistors are chosen to limit the drive current to the required level (para. 21). When the unit leaves the factory, the frequency shift is set to plus and minus 400 Hz; this may be adjusted over the range plus and minus 42 Hz to plus and minus 425 Hz, as detailed in Chapter 19.

FSK Board Links

20. LK1 is a three-position link to select positive/neutral, polar or negative/neutral (table 5) whist two-position link LK2 selects normal or reverse (where the position is dependent on the position of LK1).

Table 5: Link LK1 Settings

POSITIVE/NEUTRAL	A - D
POLAR	B - D
NEGATIVE/NEUTRAL	C - D

FSK Drive Current

21. The FSK board requires approximately 10 mA of drive current. In order to limit the drive current to this level, the values of two resistors, R1 and R2, are selected according to the telegraph supply voltage and the designated working current of the teleprinter in use. The required values are determined using the following formulae:

$$R1 = \frac{V}{(I - 10)} \text{ kilohms}$$

$$R2 = \frac{(V - 5)}{10} \text{ kilohms}$$

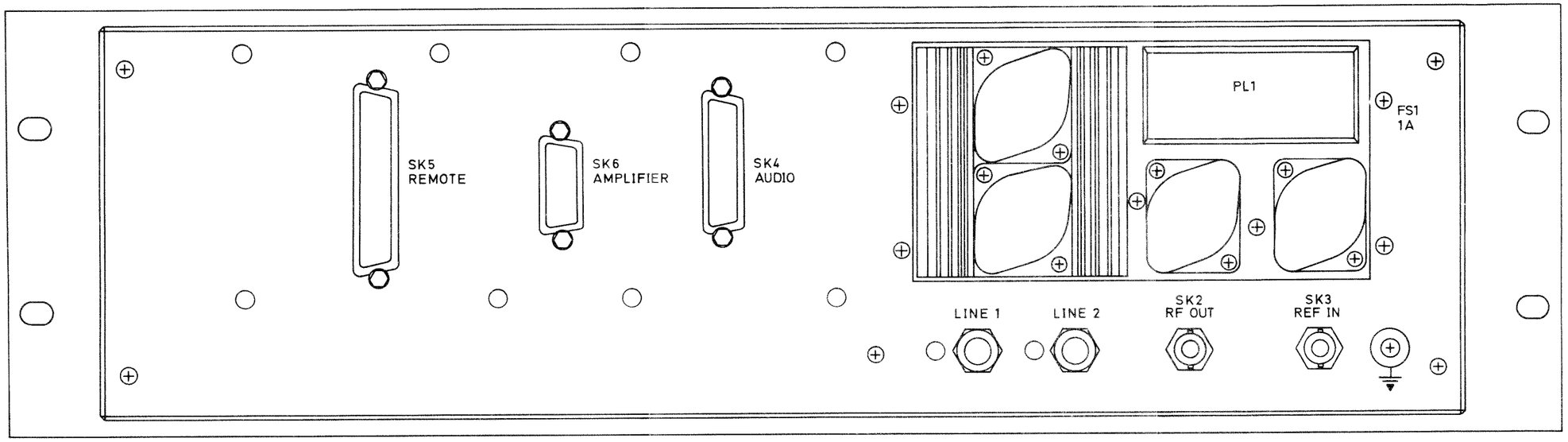
Where: V is the telegraph supply voltage (either positive or negative).

I is the designated teleprinter working current (in milliamps).

TUNE AND PILOT LEVEL ADJUSTMENT

22. The level of the RF output tuning signal and also the level of the pilot carrier are preset using the numeric pushbuttons in conjunction with switch SC on the processor board (mounted on the inner face of right-hand chassis side member), as follows:

23. (1) Set the front panel POWER switch to OFF.
(2) Set switch SC on the processor board to the ON position (in the direction of the arrow).
(3) Set the front panel POWER switch to ON.
(4) The current tune level relative to full output power is displayed in the channel number position, on the left-hand display panel. If a different level is required (1dB steps between 0 and -30 dB), press and release the TUNE pushbutton, and then press the required two numeric pushbuttons i.e. for -6dB press 0 and then 6.
(5) The current pilot carrier level relative to full output power is displayed on the right-hand display panel. If a different level is required (1 dB steps from -10 dB to -30 dB), press and release the PILOT pushbutton, and then press the two required numeric pushbuttons i.e. for -16 dB press 1 and then 6.
(6) Once the required tune and pilot levels have been preset, set the front panel POWER switch to OFF, return switch SC on the processor board to the open (down) position, and then return the POWER switch to ON.



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Rear View : MA1723

Fig.2.1

CHAPTER 3

OPERATING PROCEDURES

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Illustrations

CHAPTER 3

OPERATING PROCEDURES

INTRODUCTION

1. This chapter provides general operating instructions for the MA 1723 drive unit. For detailed operating procedures covering specific installations reference should be made to the appropriate system manuals. It is assumed that the unit has been correctly installed in accordance with the instructions given in chapter 2 and/or the appropriate system manual.

FUNCTION OF CONTROLS

2. The function of each front panel control is described in the following paragraphs; these should be read in conjunction with fig. 3.1 at the end of the chapter.

3. (1) POWER: ON/OFF toggle switch, up for ON.

(2) REMOTE: Pressing and releasing the REM pushbutton selects remote operation and a further press returns the unit to local operation. Note that remote operation is only possible when the unit is fitted with an optional remote interface board. When in the remote condition REMOTE is illuminated on the left-hand display panel. All controls are inoperative except the LINE/SET/RF switch to allow metering of the audio line level and RF output power.

(3) FREQUENCY: Pressing and releasing the FREQ pushbutton enables frequency entry via the numeric pushbuttons. ⚠ is illuminated to indicate that the displays differ from the current operating conditions. The channel and frequency display are blanked and a - cursor appears at the left-hand (most significant) frequency digit position. The required operating frequency is keyed in starting with the most significant (10 MHz) digit, and the cursor then moves to the right. After the 100 Hz digit has been keyed in, the numeric keys revert to their second function.

(4) CHANNEL: When the CHAN pushbutton is pressed and released, the last selected channel number is displayed together with the settings for that channel number. ⚠ illuminates to indicate that the displays differ from the current oprating conditions. The channel number can be changed by pressing two numeric pushbuttons (00 to 99).

The drive unit can be set to the displayed channel settings by pressing and releasing the ENTER pushbutton. Alternatively, the current operating conditions can be displayed by pressing and releasing the RCL (recall) pushbutton. After pressing two numeric pushbutton, the RCL (recall) pushbutton or the ENTER pushbutton, the numeric pushbuttons revert to their second function.

(5) RECALL: Pressing and releasing the RCL pushbutton after either FREQ or CHAN selection causes the current operating conditions (frequency and mode) to be displayed, and causes the numeric pushbuttons to revert to their second function.

(6) STORE: To store frequency and mode data in a particular channel, the information to be stored is first set up and displayed on the front panel. The STORE pushbutton is then held depressed while the two digits of the required channel number are entered. When the STORE button is released, the displayed frequency and mode data is stored in the appropriate channel.

(7) METER: The second function of the 0 numeral pushbutton. Toggles LINE and SET metering between LINE 1 and LINE 2 when ISB1 mode is in use.

(8) ENTER: The ENTER pushbutton is used to set the drive unit to the displayed settings following use of the FREQ or CHAN pushbuttons. When pressed and released it also sends a 'coarse tune initiate' signal to the associated linear amplifier, and causes the numeric pushbuttons to revert to their second function.

(9) 0 to 9: The 0 to 9 numeric keys are used to enter frequency and channel number.

(10) ISB1: The second function of the numeral 1 pushbutton. It selects ISB with USB and LSB audio from LINE 1 and LINE 2 inputs respectively.

(11) ISB2: The second function of the numeral 2 pushbutton. It selects ISB with USB audio from LINE 1 input and a TSK signal centred on 2 kHz in the lower sideband.

(12) ISB3: The second function of the numeral 3 pushbutton. It selects ISB with LSB audio from LINE 2 input and a TSK signal centred on 2 kHz in the upper sideband.

(13) STANDBY: This pushbutton selects the standby condition at the associated linear amplifier. The red indicator above the STANDBY pushbutton may be

illuminated by a signal from the associated linear amplifier when it is in the standby condition.

(14) EHT: This pushbutton is used to select the EHT ON condition (where applicable) at the associated linear amplifier. The red indicator above the EHT pushbutton may be illuminated by a signal from the linear amplifier when it is in the EHT ON condition.

(15) TUNE: Pressing and releasing the TUNE Pushbutton produces a steady RF output signal to allow manual tuning of the associated linear amplifier. The indicator above the TUNE pushbutton illuminates when the TUNE condition is selected, either manually or automatically following a change in the operating frequency, or when RESET is pressed. The level of the tune signal can be preset in 1 dB steps from 0 dB to -30 dB relative to full output power using an internal switch and the front-panel numeric pushbuttons (Chapter 2).

(16) MUTE: Pressing the MUTE pushbutton mutes the output of the drive unit and provides a mute signal for the associated linear amplifier. The indicator above the MUTE pushbutton illuminates when the mute condition is selected, either at the front panel, or externally. The mute condition is automatically entered if the drive unit synthesizer goes out of phase-lock, or if a fault is indicated in the associated linear amplifier.

(17) RESET: Pressing RESET produces an RF tuning signal and a coarse tune initiate (CTI) signal for the associated linear amplifier. This is used to reset a fault condition in the linear amplifier, denoted by the illumination of the indicator above the RESET pushbutton. When the fault has been cleared READY is illuminated in the right-hand display panel. If the fault is not cleared within two seconds after pressing RESET, the system is again muted.

(18) LOW POWER: This pushbutton is used to reduce the drive unit RF output power level to an internally preset level between 0 dB and -6 dB relative to full output power (chapter 19). The indicator above the LOW POWER pushbutton illuminates when the low power condition is selected. This pushbutton, in conjunction with numeric buttons 1 or 2 can be used to select two levels of low power on the linear amplifier. This can only be achieved if the linear amplifier has a low power select facility.

(19) USB, LSB: These pushbuttons select upper sideband or lower sideband operation respectively. The sideband selected is indicated on the right-hand display panel.

(20) PILOT: When in the USB, LSB or ISB modes, pressing PILOT selects the pilot carrier. The level of the pilot carrier can be preset in 1 dB steps from -10 dB to -30 dB relative to full carrier level using an internal switch and the front-panel numeric pushbuttons (Chapter 2). This preset carrier level is then recalled whenever PILOT is selected.

(21) AM: This pushbutton selects carrier and upper sideband, both at a level of -6 dB relative to peak envelope power.

(22) CW: When this pushbutton is pressed and released, it enables the rear panel KEY input. Full carrier is transmitted when the key is held down.

(23) FSK: Pressing and releasing the FSK pushbutton enables the FSK input at the rear panel. A TSK signal centred on 2 kHz is transmitted in the upper sideband and the synthesizer is shifted by 2 kHz so that at the drive unit output the FSK signal is centred on the tuned frequency. The tone shift is internally preset within the range plus and minus 42 Hz to plus and minus 425 Hz.

(24) LINE/SET/RF Switch: This three-position switch selects the function of the meter, displayed in the right-hand display panel. In the LINE position, the incoming audio line signals can be monitored. In the SET position, the rear-panel line level potentiometer can be set for a 0 dB meter reading. In the RF position, an indication of the drive unit RF output power level is provided.

(25) VOX/PTT/TX switch: This three position switch selects either VOX (voice operated transmission), PTT (press-to-talk) or TX (continuous transmit).

FRONT PANEL INDICATORS

4. (1) CHANNEL: Indicates the channel number when in the channel mode, or the test number when in the self-test mode. Also used to indicate the TUNE level during the preset tune level procedure (Chapter 2).

(2)  This symbol is displayed to indicate that the drive unit operating parameters may be different from those displayed.

(3) FREQUENCY: Indicates the operating frequency in kHz. Can also indicate error codes when in the self-test mode (para. 21).

(4) REMOTE: Indicates that remote operation has been selected.

(5) PILOT dB: Indicates the preset pilot carrier level, in dB, relative to full output power.

(6) METER: Indicates RF output level or audio input levels depending on the position of the LINE/SET/RF switch.

(7) MODES: Indicate the selected transmitting modes.

(8) READY: Indicates that the drive unit has received a READY signal from the associated linear amplifier.

(9) TRANSMIT: Indicates that the drive unit is in the transmit state.

(10) FAULT: Indicates that the synthesizer and/or the reference generator is out of lock.

(11) RED PWR: Indicates a reduced power condition at the associated linear amplifier.

(12) STANDBY LED: When illuminated, this LED indicates that the associated linear amplifier is in the standby condition.

(13) EHT LED: When illuminated, this LED indicates that the associated linear amplifier has EHT selected.

(14) TUNE LED: When illuminated, this LED indicates that the drive unit is providing a continuous RF output signal for tuning purposes.

(15) MUTE LED: When illuminated, this LED indicates that the drive unit is in the mute condition, due to manual or external mute selection.

(16) RESET LED: When illuminated, this LED indicates an external fault (within the associated linear amplifier) is present.

(17) LOW POWER LED: This LED is illuminated when LOW POWER is selected.

OPERATING PROCEDURES

5. The procedures for frequency entry, mode selection, channel operation, recall operation, enter operation and remote operation are given in the following paragraphs. Before attempting to operate the drive unit, it is important to note that when it is operating in the ⚠ mode (⚠ symbol displayed), the front panel display may not indicate the drive unit operating frequency and mode.

FREQUENCY ENTRY

6. To enter a frequency, press and release the FREQ pushbutton. This selects the display only mode (⚠ displayed), sets the frequency display to zero, and enters a - prompt in the 10 MHz digit position. The numeric pushbuttons are enabled, and if 0, 1 or 2 is pressed, the digit is displayed in the 10 MHz digit and the prompt moves one position to the right. If the first digit pressed is in the range 3 to 9, it is ignored as the highest operating frequency available is 29999.9 kHz. The numeric pushbuttons are now used to enter the remainder of the required operating frequency, and the prompt moves to the right after each entry. When all six digits have been correctly entered, the prompt disappears and further numeric entries are ignored. If, during a frequency entry (i.e. before the prompt disappears), a non-numeric pushbutton other than ENTER, RCL or a transmitter function pushbutton (STANDBY, EHT, TUNE, MUTE, RESET, LOW POWER) is pressed, a zero is entered into the prompt position and the frequency entry mode is terminated. In the case of a transmitter function pushbutton, frequency entry is not affected and continuation is possible.

7. If, during frequency entry, an error is made, i.e. the wrong numeral button is pressed, press and release the FREQ pushbutton and start again. To set the drive unit to the new frequency, press and release the ENTER pushbutton. Any unentered digits of the operating frequency are set to zero (thus trailing zeros need not be entered), and the drive unit is then muted for approximately 100 milliseconds to allow the synthesizer to settle before the coarse tune initiate signal is produced. If the associated linear amplifier tunes correctly, a READY signal is sent back to the drive unit, and READY is illuminated on the right-hand display panel. The tune signal is then removed (unless manual tune is selected) and normal operation is restored. A tuning failure at the associated linear amplifier may result in the transfer of a fault ignal to the drive unit, and this is indicated by the illumination of the RESET LED.

MODE SELECTION

8. The required mode is selected by pressing and releasing the appropriate mode pushbutton (USB, LSB, PILOT, AM, CW, FSK, ISB1, ISB2, ISB3). If PILOT is selected without previously selecting USB, LSB or ISB, the selection is ignored. If the unit is in the display-only mode i.e. ⚠ is displayed, the new mode will only be entered after the ENTER pushbutton is pressed and released.

CHANNEL OPERATION

9. To enter the display-only channel mode, press and release the CHAN pushbutton. The parameters and channel number of the last channel to be accessed are displayed, together with the ⚠ symbol to indicate that the displays do not indicate the current operating parameters. Two numeric pushbuttons may now be pressed, in turn, to display the parameters of a different channel number. After two numeric pushbuttons have been pressed, the numeric pushbuttons revert to their second function, so to select a different channel number, the CHAN pushbutton must first be pressed and released again. To set the drive unit to the displayed channel parameters, press and release the ENTER pushbutton. To restore the front panel displays to the current operating parameters, press and release the RCL pushbutton.

NOTE: Only channels that contain stored frequency and mode data can be recalled. If a non-programmed channel number is selected following operation of the CHAN pushbutton, the selection is ignored.

10. To store the displayed frequency and mode settings into a particular channel, press and hold the STORE pushbutton. The word CHANNEL is displayed (if not already displayed) and any previously displayed channel number is blanked. Now use the numeric pushbuttons to select the required channel number (00 to 99), most significant digit first, and then release the STORE key. If the store operation fails, the channel number is displayed, and the frequency and mode displays are blanked. Selecting a new frequency and mode will return the unit to normal operation.

RECALL OPERATION

11. The RECALL pushbutton is used to cancel the display-only mode (⚠ displayed) and to display the current operating parameters.

ENTER OPERATION

12. The ENTER pushbutton is used, when in the display-only mode (⚠ displayed), to set the drive unit to the displayed parameters.

REMOTE OPERATION

13. The REMOTE pushbutton is used to transfer control to a remote unit. The word REMOTE is displayed (left-hand display panel) and in this condition the front panel controls apart from the LINE/SET/RF metering switch are disabled. A further press of the REMOTE pushbutton extinguishes the REMOTE indication and returns the unit to local control.

14. The REMOTE pushbutton is also used to select a self test routine, as described in para. 23.

TRANSMITTER SELECTION

STANDBY Pushbutton

15. Selecting STANDBY routes a control signal to the associated linear amplifier to select the standby condition. The revertive information from the linear amplifier is used to illuminate the LED above the STANDBY pushbutton. A further press of the STANDBY pushbutton toggles the control signal to switch off the standby condition.

EHT Pushbutton

16. The EHT pushbutton toggles a control signal which is routed to the linear amplifier to switch the EHT supply, provided STANDBY has already been selected.

TUNE Pushbutton

17. This pushbutton toggles the tune status. When selected, a continuous unmodulated carrier, at the selected operating frequency and at a preset amplitude level, is produced at the RF OUT connector on the rear panel.

MUTE Pushbutton

18. Pressing this pushbutton toggles the mute function. When MUTE is selected (indicated by the illumination of LED above the MUTE pushbutton), the drive unit sends a mute signal to the associated linear amplifier, the drive unit RF output is muted, and the audio input circuit is open-circuited.

LOW POWER Pushbutton

19. This pushbutton toggles the low power select circuit. When LOW POWER is selected (indicated by the illumination of the LED above the LOW POWER pushbutton), the drive unit RF output is reduced to a preset level (Chapter 19). The LOW POWER pushbutton is disabled when manual TUNE is selected. For linear amplifiers with a low power facility, two levels of low power can be achieved. To do this, press and hold down the low power pushbutton, then press and release numeric pushbutton 1 or 2. Finally release the low power button.

When used in conjunction with the TA 1823 linear amplifier, with the low power select facility, pressing button 1 gives 500 W output (nominal) and 2 gives 250 W output (nominal). To regain full power (1000 W for the TA 1823) just press and release the low power pushbutton only.

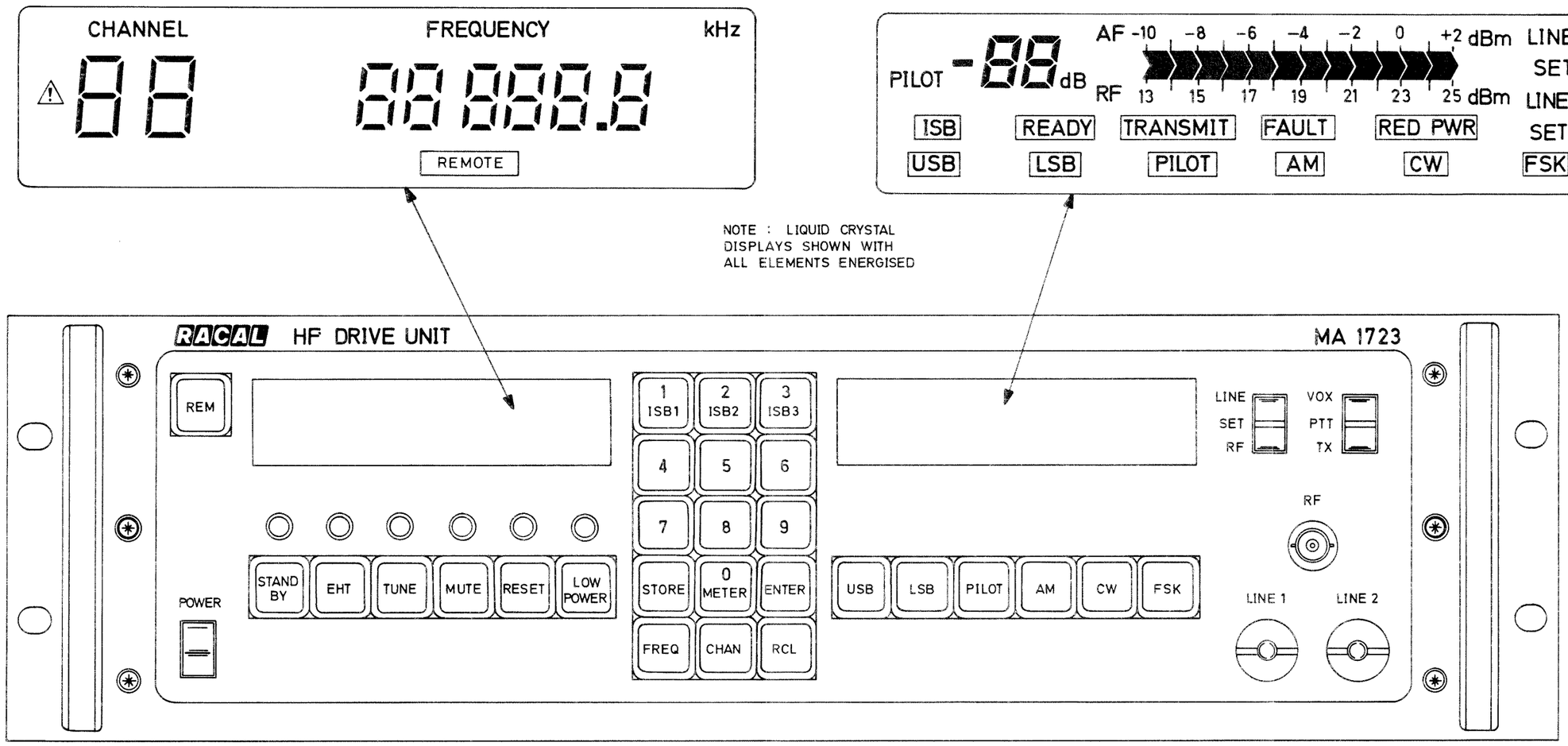
N.B. Power levels may be set by presets on the TA 1823 ALC card.

RESET Pushbutton

20. Provided MUTE is not selected, pressing the RESET pushbutton generates the coarse tune initiate (CTI) signal.

SELF TEST ROUTINES

21. The MA 1723 contains a number of self-test routines. These are used, together with other procedures, to functionally test the unit and to assist in the location of a fault (chapers 18, 19 and 20). To enter the self-test mode, ensure that the unit is not in the display-only mode (⚠ not illuminated), press and hold the REM pushbutton, press and release the numeral 0 pushbutton twice, and then release the REM pushbutton. The test number is displayed in the channel number position, and various other indicators are used to indicate the pass or failure of the test. For further details, refer to chapter 18. To exit from the self-test mode, press and release the RCL pushbutton.



Front Panel Controls and Indicators

Fig. 3·1

CHAPTER 4

FRONT PANEL DISPLAY BOARD

CONTENTS

Illustrations

CHAPTER 4

FRONT PANEL DISPLAY BOARD

INTRODUCTION

1. This board is mounted on the inner face of the front sub-panel and accommodates the two liquid-crystal display panels with associated drivers, the 28 front panel pushbutton switches and the six LED status indicators. It also forms the interface for the remaining front panel controls and connectors apart from the POWER ON/OFF switch and the RF monitor socket.

CIRCUIT DESCRIPTION (fig. 4.1)

Switch Matrix

2. The 28 front-panel, spring-loaded, single make-contact pushbutton switches, SA to SAF, are connected as a four-column by eight-row matrix which is continually read by the processor via additional circuitry located on the front panel interface board (Chapter 5).

Display Oscillator

3. The liquid crystal display driver devices (ML2 to ML9, ML12 to ML21, ML24 and ML25) require a low-frequency squarewave input signal. This signal is produced by ML23 which is connected as an astable multivibrator and runs at a nominal frequency of 130 Hz (timing components R12, C9). The Q output signal (TP4) is connected in parallel to the DF (display frequency) input pin of each display driver device.

Numeric Displays

4. The numeric displays, i.e. the frequency, channel number and pilot carrier level displays, are all driven by a number of BCD-to-seven segment C-MOS latched decoder/driver devices ML8, ML9 and ML13 to ML21. These devices decode the applied 1-2-4-8 BCD input signals to provide the required 7-segment output signals which are produced at the a to g output pins when a positive voltage is applied to the strobe input. When a '0' is present at the strobe input, the data is latched at the a to g output pins. When the DF input is at '0', the selected segment output signals are at a '1' level, and when the DF input is at '1', the selected segment output signals are at a '0' level. Since a nominal 130 Hz squarewave signal is present at the DF input, the selected segments will have a squarewave output that is 180 degrees out-of-phase with the DF input, whilst those segments that are not selected will have a squarewave output that is in-phase with the DF input. Since the DF signal is also applied to the common return (and unused) pins of the display devices (ML1 and ML11), only the segments that are selected will be illuminated.

Non-Numeric Displays

5. The remaining (non-numeric) displays are driven by a number of 4-segment C-MOS display driver devices ML2 to ML7, ML12, ML24 and ML25. These devices are similar in operation to the 7-segment devices except that individual strobe inputs are provided for each segment. In this application however, the four strobe inputs of each device are commoned.

Display Strobes

6. The strobe signals for the display driver devices are produced by ML10 which consists of a 4-bit latch and a 4-line to 16-line decoder. The latch facility however, is not used (strobe input connected to +5 V), and the device is simply used as an address decoder. When a '1' is present at the inhibit input, all the strobe outputs are at '0'; when a '0' is present at the inhibit input, a '1' is produced at the addressed strobe output.

Status Indicators

7. The S15 strobe signal from ML10 is also used to clock hex D-type flip-flop ML26 to control the illumination of the LED status indicators D1 to D6 via open-collector NAND buffer/driver stages ML27, ML28 and ML29.

Microphone Preamplifiers

8. ML22 is a dual MOS/FET-input operational amplifier, connected as two identical buffer/amplifiers for microphone inputs 1 and 2. A dc energising supply for carbon-type microphones is provided via R1 and R4 for MIC1, R2 and R6 for MIC2.

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
		FRONT PANEL DISPLAY BOARD (ST81643)			
Resistors					
R1	100	Metal Oxide		2	910388
R2	100	Metal Oxide		2	910388
R3	10k	Metal Oxide		2	914042
R4	100	Metal Oxide		2	910388
R5	10k	Metal Oxide		2	914042
R6	100	Metal Oxide		2	910388
R7	10k	Metal Oxide		2	914042
R8	10k	Metal Oxide		2	914042
R9	33k	Metal Oxide		2	913495
R10	33k	Metal Oxide		2	913495
R11	100	Metal Oxide		2	910388
R12	15k	Metal Oxide		2	920645
R13	330	9-Resistor SIL Network		2	939890
Capacitors			V		
C1	6µ8	Tantalum Bead	35	20	923573
C2	0µ1	Polycarbonate	100	10	931130
C3	0µ1	Polycarbonate	100	10	931130
C4	6µ8	Tantalum Bead	35	20	923573
C5	47	Electrolytic	40	+50-10	941842
C6	47	Electrolytic	40	+50-10	941842
C7	6µ8	Tantalum Bead	35	20	923573
C8	100	Electrolytic	40	+50-10	940766
C9	0µ1	Polycarbonate	100	10	931130
C10	6µ8	Tantalum Bead	35	20	923573
Connectors					
PL44		Plug, 13-way			939889
SK41		Cable Assembly			BA82565
		Comprising:-			
		Connector, PCB, 50-way			940002
		Socket, 50-way			934824
		Cable, flat, 50-way			931534
		Clamp, strain relief			934815
Switches					
SA to SAF		Switch, key			938467

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number

Switch Keytops

Keytop	Part No.	Keytop	Part No.	Keytop	Part No.
4	BD81103/28	RCL	BD81103/54	RESET	BD81103/76
5	BD81103/29	TUNE	BD81103/55	PILOT	BD81103/77
6	BD81103/30	REM	BD81103/57	FSK	BD81103/78
7	BD81103/31	STORE	BD81103/58	FREQ	BD81103/79
8	BD81103/32	LSB	BD81103/60	1/ISB 1	BD81103/81
9	BD81103/33	USB	BD81103/61	2/ISB 2	BD81103/82
ENTER	BD81103/36	LOW POWER	BD81103/72	3/ISB 3	BD81103/83
AM	BD81103/45	STANDBY	BD81103/73	0/METER	BD81103/84
CW	BD81103/47	EHT	BD81103/74		
CHAN	BD81103/53	MUTE	BD81103/75		

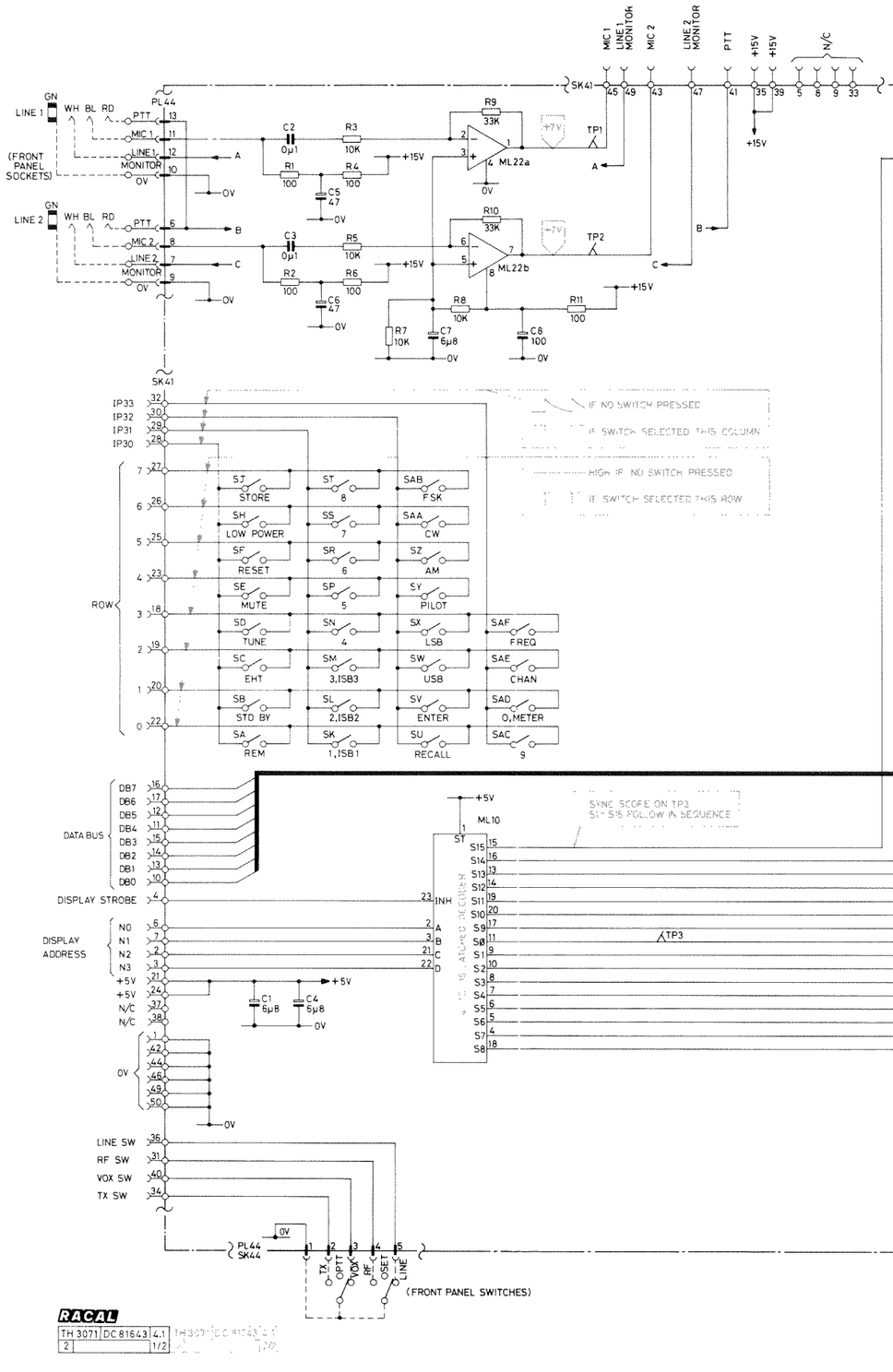
Diodes

D1 to D6	LED, Red HP5082-4650	929360

Integrated Circuits

ML1	LCD Display Panel	CD80542
ML2	4-segment LCD Driver 4054	930994
ML3	4-segment LCD Driver 4054	930994
ML4	4-segment LCD Driver 4054	930994
ML5	4-segment LCD Driver 4054	930994
ML6	4-segment LCD Driver 4054	930994
ML7	4-segment LCD Driver 4054	930994
ML8	7-segment LCD Driver 4056	930996
ML9	7-segment LCD Driver 4056	930996
ML10	4 to 16 line decoder 4514	931010
ML11	LCD Display Panel	C08181
ML12	4-segment LCD Driver 4054	930994
ML13	7-segment LCD Driver 4056	930996
ML14	7-segment LCD Driver 4056	930996
ML15	7-segment LCD Driver 4056	930996
ML16	7-segment LCD Driver 4056	930996
ML17	7-segment LCD Driver 4056	930996
ML18	7-segment LCD Driver 4056	930996
ML19	7-segment LCD Driver 4056	930996
ML20	7-segment LCD Driver 4056	930996

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Integrated Circuits (Continued)					
ML21		7-segment LCD Driver 4056			930996
ML22		Dual Operational Amplifier 3240			933580
ML23		Multivibrator 4047			930992
ML24		4-segment LCD Driver 4054			930994
ML25		4-segment LCD Driver 4054			930994
ML26		Hex D-type flip-flop 40174			931060
ML27		Dual 2-input NAND buffer 40107			931052
ML28		Dual 2-input NAND buffer 40107			931052
ML29		Dual 2-input NAND buffer 40107			931052
Miscellaneous					
		Test Points			936148
		8-pin DIL IC socket			940901
		14-pin DIL IC socket			940902
		16-pin DIL IC socket			940903
		24-pin DIL IC socket			930609
		20-pin SIL socket			938468
		25-pin SIL socket			938469



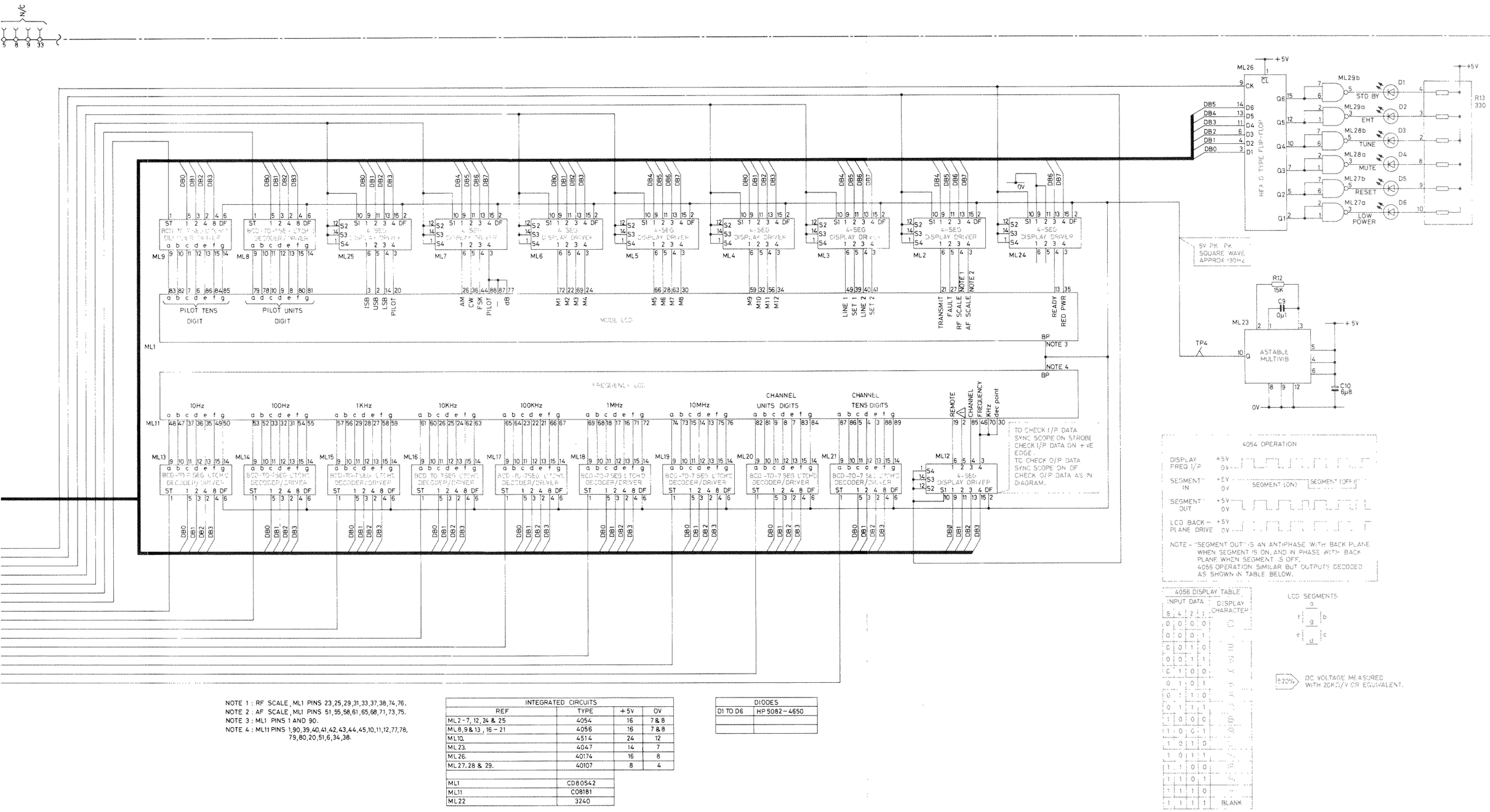
NOTE 1 : RF SCALE, ML1 PINS 23,25,29,31,33,37,38,74,76.
NOTE 2 : AF SCALE, ML1 PINS 51,55,58,61,65,68,71,73,75.
NOTE 3 : ML1 PINS 1 AND 90.
NOTE 4 : ML11 PINS 1,90,39,40,41,42,43,44,45,10,11,12,77,78, 79,80,20,51,6,34,38.

INTEGRATED CIRCUITS			
REF	TYPE	+5V	0V
ML2 - 7, 12, 24 & 25	4054	16	7 & 8
ML8, 9 & 13, 16 - 21	4056	16	7 & 8
ML10.	4514	24	12
ML23.	4047	14	7
ML26.	40174	16	8
ML27, 28 & 29.	40107	8	4
ML1	CD80542		
ML11	C08181		
ML22	3240		

DIODES	
D1 TO D6	HP 5082 - 4650

RACAL

TH 3071	DC 81643	4.1	
2		1/2	

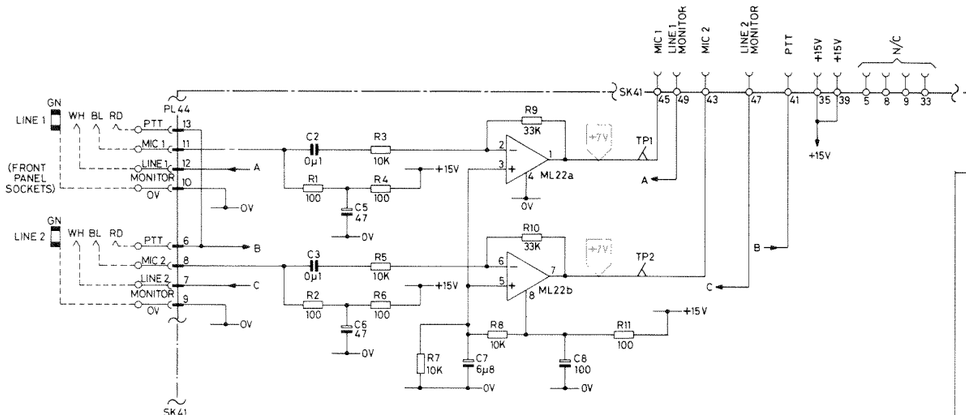


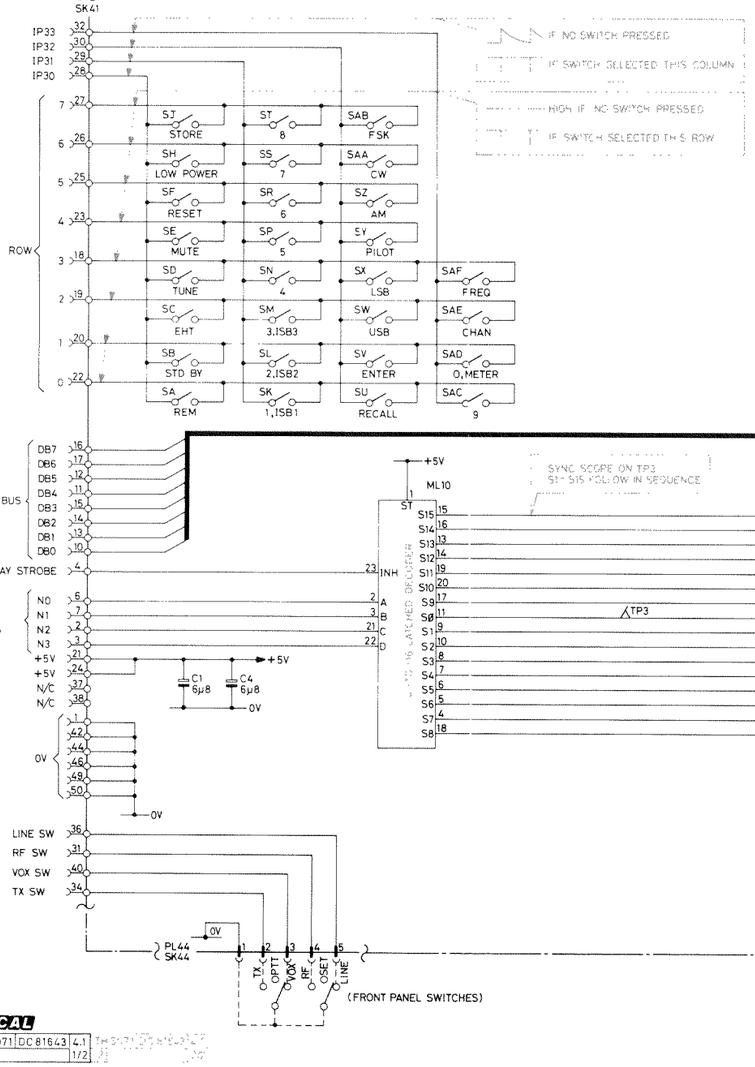
NOTE 1 : RF SCALE, ML1 PINS 23,25,29,31,33,37,38,74,76.
NOTE 2 : AF SCALE, ML1 PINS 51,55,58,61,65,68,71,73,75.
NOTE 3 : ML1 PINS 1 AND 90.
NOTE 4 : ML11 PINS 1,90,39,40,41,42,43,44,45,10,11,12,77,78, 79,80,20,51,6,34,38.

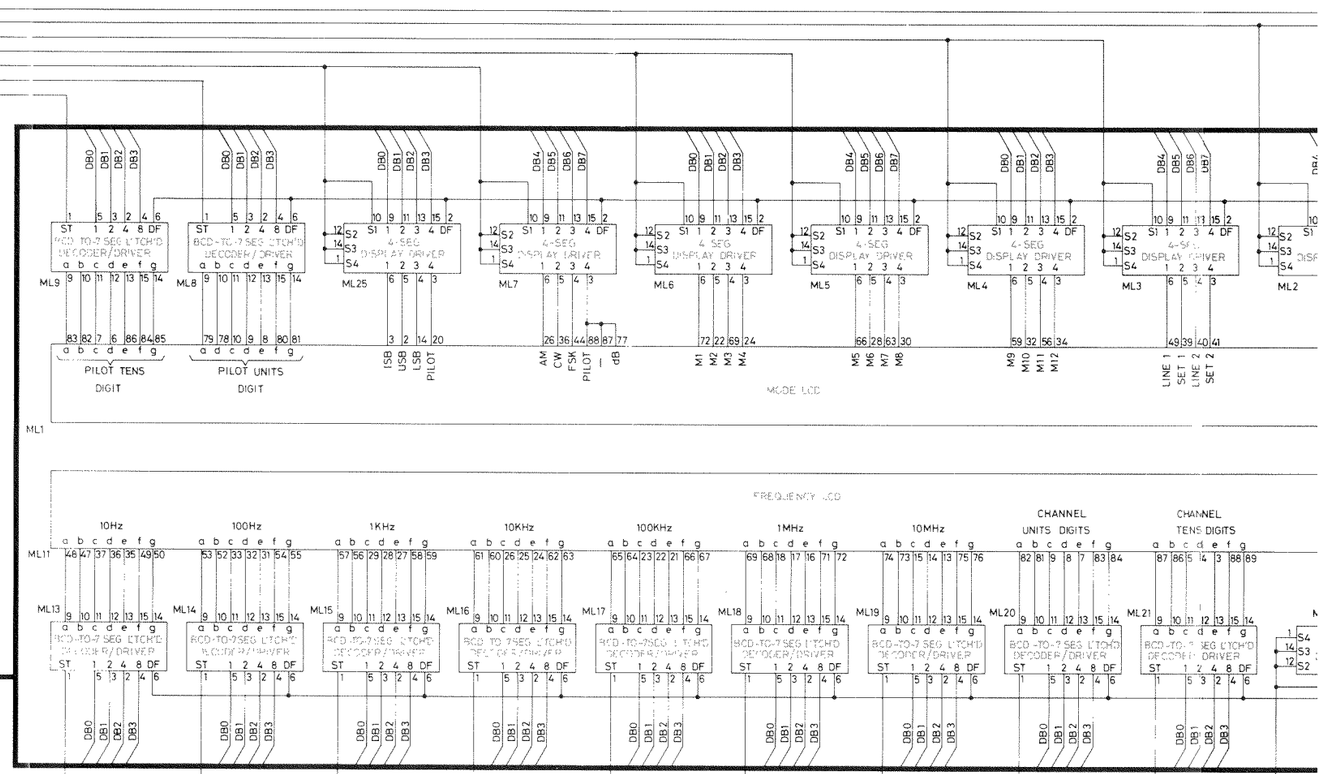
INTEGRATED CIRCUITS			
REF	TYPE	+5V	0V
ML2-7, 12, 24 & 25	4054	16	7 & 8
ML8, 9 & 13, 16-21	4056	16	7 & 8
ML10.	4514	24	12
ML23.	4047	14	7
ML26.	40174	16	8
ML27, 28 & 29.	40107	8	4
ML1	CD80542		
ML11	C08181		
ML22	3240		

DIODES	
D1 TO D6	HP 5082-4650

Circuit : Front Panel Display Board Fig. 4.1







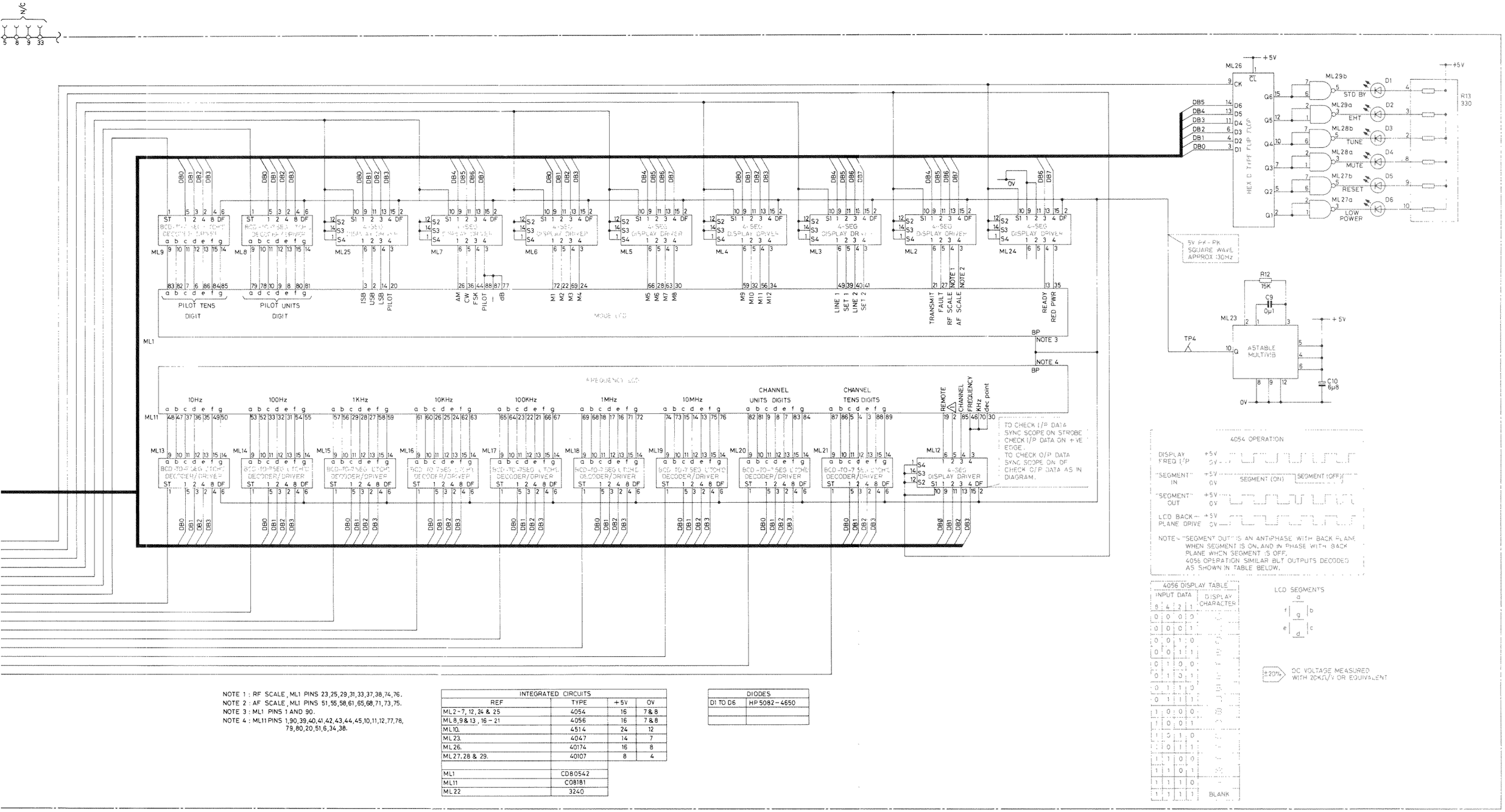
NOTE 1 : RF SCALE, ML1 PINS 23,25,29,31,33,37,38,74,76.
NOTE 2 : AF SCALE, ML1 PINS 51,55,58,61,65,68,71,73,75.
NOTE 3 : ML1 PINS 1 AND 90.
NOTE 4 : ML11 PINS 1,90,39,40,41,42,43,44,45,10,11,12,77,78, 79,80,20,51,6,34,38.

INTEGRATED CIRCUITS			
REF	TYPE	+5V	0V
ML2-7, 12, 24 & 25	4054	16	7 & 8
ML8, 9 & 13, 16 – 21	4056	16	7 & 8
ML10.	4514	24	12
ML23.	4047	14	7
ML26.	40174	16	8
ML27, 28 & 29.	40107	8	4
ML1	CD80542		
ML11	C08181		
ML22	3240		

DIODES	
D1 TO D6	HP 5082 – 4650

RACAL

TH 3071	DC 81643	4.1
2		1/2



4054 OPERATION

DISPLAY FREQ I/P	+5V / 0V	
"SEGMENT" IN	+5V / 0V	SEGMENT (ON) / SEGMENT (OFF)
"SEGMENT" OUT	+5V / 0V	
LCD BACK-PLANE DRIVE	+5V / 0V	

NOTE - "SEGMENT OUT" IS AN ANTIPHASE WITH BACK PLANE WHEN SEGMENT IS ON, AND IN PHASE WITH BACK PLANE WHEN SEGMENT IS OFF. 4056 OPERATION SIMILAR BUT OUTPUTS DECODED AS SHOWN IN TABLE BELOW.

4056 DISPLAY TABLE

INPUT DATA 8	4	2	1	DISPLAY CHARACTER
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	BLANK

LCD SEGMENTS: a, b, c, d, e, f, g

±20% DC VOLTAGE MEASURED WITH 20KΩ/V OR EQUIVALENT

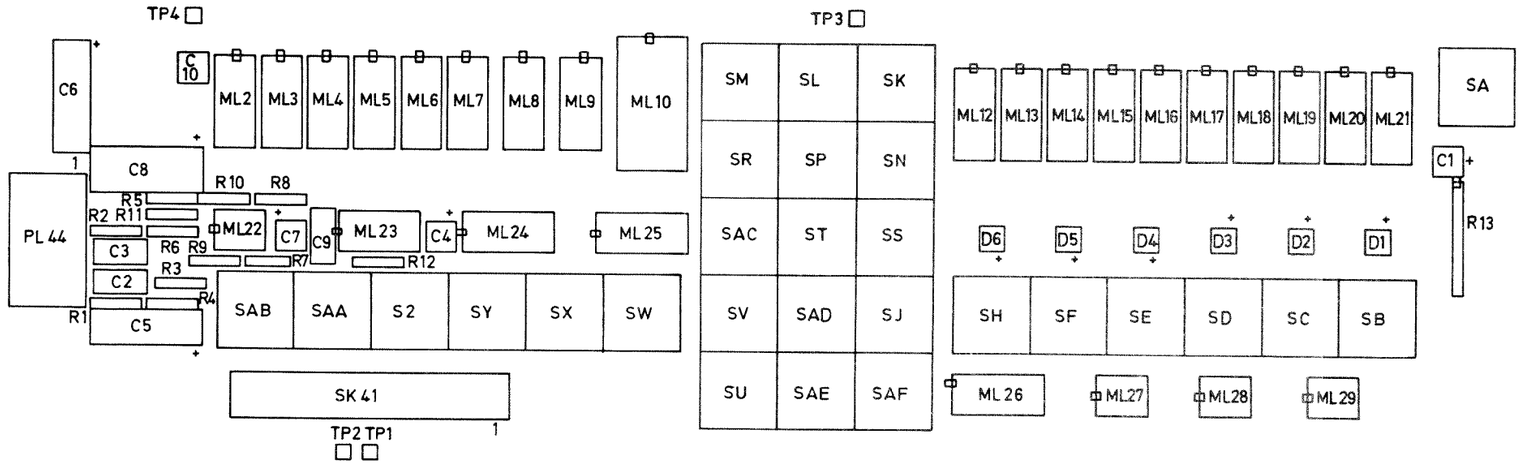
NOTE 1 : RF SCALE, ML1 PINS 23,25,29,31,33,37,38,74,76.
NOTE 2 : AF SCALE, ML1 PINS 51,55,58,61,65,68,71,73,75.
NOTE 3 : ML1 PINS 1 AND 90.
NOTE 4 : ML11 PINS 1,90,39,40,41,42,43,44,45,10,11,12,77,78, 79,80,20,51,6,34,38.

INTEGRATED CIRCUITS			
REF	TYPE	+5V	0V
ML2-7, 12, 24 & 25	4054	16	7 & 8
ML 8, 9 & 13, 16 – 21	4056	16	7 & 8
ML10.	4514	24	12
ML23.	4047	14	7
ML26.	40174	16	8
ML27, 28 & 29.	40107	8	4
ML1	CD80542		
ML11	C08181		
ML22	3240		

DIODES	
D1 TO D6	HP 5082-4650

Circuit : Front Panel Display Board

Fig. 4.1



RACAL

TH 3071	DA 8164 2/5
1	

Layout: Front Panel Display Board

Fig 4.2

CHAPTER 5

FRONT PANEL INTERFACE BOARD

CONTENTS

Tables

Illustrations

CHAPTER 5

FRONT PANEL INTERFACE BOARD

INTRODUCTION

1. This board is mounted on the front sub-panel and forms the interface between the processor board and the synthesizer, reference generator, modulation, front panel display and rear panel boards. It is also used as the distribution board between these same boards and the power supply module. Note that connections between the processor board and the optional remote interface board are made direct, and that direct connections also exist between the power supply module and the RF output amplifier board, the mixer board and the frequency standard module (see chap. 16).

CIRCUIT DESCRIPTION (fig. 5.1)

Input Data Strobe Decoder

2. A negative-going strobe pulse from the processor board, at PL39 pin 9, is routed via 8-channel demultiplexer device ML6 to a number of stages for the transfer of data to the processor data bus, for addresses in the range hexadecimal 30 to 37 at the PA address bus (table 1). Note that because the PA5 address bus line is not decoded the addresses given are not uniquely defined.

Table 1 : Input Data Strobes

PA ADDRESS BUS									STROBED INPUT DATA
HEX	7	6	5	4	3	2	1	0	
30	0	0	1	1	0	0	0	0	) PUSHBUTTON
31	0	0	1	1	0	0	0	1	) SWITCH
32	0	0	1	1	0	0	1	0	) DATA
33	0	0	1	1	0	0	1	1	)
34	0	0	1	1	0	1	0	0	RF/SET/LINE SWITCH
35	0	0	1	1	0	1	0	1	TX/PTT/VOX SWITCH
36	0	0	1	1	0	1	1	0	NOT USED
37	0	0	1	1	0	1	1	1	LINEAR AMPLIFIER STATUS

3. With the PA7 and PA6 lines both at '0' (table 1), a '0' is produced at the output of exclusive OR gate G1, and with a '1' at the PA4 line, the output of exclusive OR gate G2 is also at a '0'. Thus for hexadecimal addresses in the range 30 to 37, the output of OR gate G3 is at a '0' to remove the inhibit condition from ML6, whilst ML9 is inhibited by the '1' output of OR gate G4. The levels present at the PA0, PA1 and PA2 lines are then decoded by ML6 and the negative-going strobe signal at the X input is routed to the appropriate output pin.

Pushbutton Switch Data

4. Addresses 30 to 33 are applied in turn to route the strobe pulse, in turn, to the four columns of the pushbutton switch matrix (on the front panel display board - chap. 4) via PL41 pins 28, 29, 30 and 32. Since for these addresses the PA2 line is at '0' (table 1), the strobe pulse is also routed via OR gates G5 and G6 to tri-state buffers ML12b and ML13b to route the resulting pushbutton switch matrix row data to the processor board via the data bus. The switch data is listed in table 2.

Table 2 : Pushbutton Switch Data

DATA BUS	PA ADDRESS BUS (HEX)			
	30	31	32	33
DB0	REM	1 ISB 1	RECALL	9
DB1	STD BY	2 ISB 2	ENTER	0, METER
DB2	EHT	3 ISB 3	USB	CHAN
DB3	TUNE	4	LSB	FREQ
DB4	MUTE	5	PILOT	
DB5	RESET	6	AM	
DB6	LOW POWER	7	CW	
DB7	STORE	8	FSK	

RF/SET/LINE Switch Data

5. Hexadecimal address 34 at the PA bus routes the strobe to tri-state buffers ML2 and ML12a to allow examination of the RF/SET/LINE switch setting, and also the 'FSK fitted' line; this line is taken via the rear panel board to the FSK board connector, and is automatically connected to OV when the optional FSK board is fitted to the unit. The coding of the relevant data bus lines is given in table 3.

Table 3 : RF/SET/LINE Switch Data

DATA BUS	ADDRESS 34
0	RF SWITCH
1	LINE SWITCH
2	FSK FITTED
3	)
4	)
5	) NOT USED
6	)
7	)

TX/PTT/VOX Switch Data

6. The negative-going strobe pulse at the 35 output of ML6 enables tri-state buffers ML13a and ML15 to allow examination of the TX/PTT/VOX switch setting as well as the state of the external mute line, the external PTT line and AGC select lines (table 4).

Table 4 : TX/PTT/VOX Switch Data

DATA BUS	ADDRESS 35
0	EXTERNAL PTT
1	EXTERNAL MUTE
2	VOX SWITCH
3	TX SWITCH
4	VOX
5	NOT USED
6	LSB AGC ON
7	USB AGC ON

Linear Amplifier Status

7. Status information from the associated linear amplifier is applied to SK6 on the rear panel and is then routed to the front panel interface board via the rear panel board and PL43 pins 11 to 16. Transistor TR1 is normally on, and is turned off for the duration of the strobe pulse at TP1 when address 37 is present on the PA address bus. Thus a '0' from TR1 is normally applied to one input of open-collector NAND buffers G9 to G14, allowing the outputs to be pulled up to a '1' by the appropriate resistors of network R1. When address 37 is subsequently applied to the PA bus, the negative-going strobe pulse turns off TR1, and any OV status input signal is inverted by the appropriate NAND buffer to route a '1' to the processor board. The coding of the data bits is given in table 5.

Table 5 : Linear Amplifier Status Data

DATA BUS	ADDRESS 37
0	FAULT
1	READY
2	EHT ON
3	STANDBY ON
4	REDUCED POWER
5	MATRIX INTERLOCK

Output Data Strobe Decoder

8. A 4-to-16 line decoder ML9 is used to produce a number of output data strobes (table 6) to route data from the processor data bus. This stage responds to hexadecimal addresses in the range 20 to 2F applied to the PA bus; these are dedicated addresses, but because the PA5 line is not decoded, they are not uniquely defined.

Table 6 : Output Data Strobes

PA ADDRESS BUS									OUTPUT STROBE FUNCTION
HEX	7	6	5	4	3	2	1	0	
20	0	0	1	0	0	0	0	0	FRONT PANEL
21	0	0	1	0	0	0	0	1	DISPLAYS
22	0	0	1	0	0	0	1	0	D-A CONVERTER
23	0	0	1	0	0	0	1	1	NOT USED
24	0	0	1	0	0	1	0	0	LINEAR AMPLIFIER
25	0	0	1	0	0	1	0	1	CONTROL
26	0	0	1	0	0	1	1	0	NOT USED
27	0	0	1	0	0	1	1	1	
28	0	0	1	0	1	0	0	0	
29	0	0	1	0	1	0	0	1	SYNTHESIZER BOARD
2A	0	0	1	0	1	0	1	0	MODULATION BOARD
2B	0	0	1	0	1	0	1	1	
2C	0	0	1	0	1	1	0	0	
2D	0	0	1	0	1	1	0	1	NOT USED
2E	0	0	1	0	1	1	1	0	NOT USED
2F	0	0	1	0	1	1	1	1	METERED FUNCTION

9. The '0' at the PA4 line (table 6) results in a '1' at the output of G3, and ML6 is therefore inhibited for addresses in the range 20 to 2F. The inhibit condition is removed from ML9 for the duration of the negative-going strobe pulse at TP1, and the levels at the PA0 to PA3 address bus lines are decoded to produce a positive-going strobe pulse at the appropriate output pin.

Front Panel Displays

10. The front panel displays are all updated approximately every 50 milliseconds. At the beginning of each display sequence, the presettable binary counter ML7 is preset to zero (P1 to P4 inputs set to zero via the data bus, and address 21 applied to preset-enable the device). The Q1 to Q4 outputs of ML7, and hence the N0 to N3 inputs of the 4-line to 16-line decoder on the front panel display board, are set to the zero state, and address 20 is then applied to ML9 to produce a negative-going display strobe pulse at the output of G7. Since the positive-going edge of this strobe pulse is used to clock ML7, the remaining displays are updated simply by continually applying address 20 until ML7 reaches a count of 15. The displays updated for each state of ML7 are listed in table 7.

Table 7 : Display Data

ML7 COUNT STATE	DISPLAYS UPDATED	
0	10 Hz)	
1	100 Hz)	
2	1 kHz)	
3	10 kHz)	FREQUENCY
4	100 kHz)	
5	1 MHz)	
6	10 MHz)	
7	UNITS)	CHANNEL
8	TENS)	NUMBER
9	TENS)	PILOT
A	UNITS)	CARRIER
B	MODES	
C	METER SEGMENTS	
D	METER SEGMENTS, LINE/SET	
E	METER SCALE, CHANNEL, FREQ, FAULT	
F	LEDS, READY, REDUCED POWER	

D-A Converter

11. The digital-to-analogue converter stage ML10 is used, in conjunction with 4-bit latch ML3, voltage level shifter ML4 and 16-way analogue multiplexer ML11, for metering purposes. Of the 16 analogue signals applied to ML11 (listed in table 8) four only, namely AC meter (audio level), DC meter (detected RF output level), synthesizer varactor voltage and 20 MHz varactor voltage, are regularly monitored by the processor. The remaining analogue signals are monitored as part of the built-in self-test routines described in chapter 18.

Table 8 : Metered Analogue Signals

Code	Signal
00	Synthesizer Board RF Output Level
01	Synthesizer Board Varactor Voltage
02	1.4 MHz Level
03	20 MHz Varactor Voltage
04	40 MHz Level
05	AC Meter (Audio Level)
06	DC Meter (Detected RF Level and AGC Voltage)
07	RF output Level (RF Output Board)
08	Mixer Board Output Level
09	Not Used
0A	+5V)
0B	+15V) Approximately 5V
0C	-15V) levels from
0D	+20V) supply metering
0E	+12V) attenuators
0F	-30V)

12. To measure a particular signal, the appropriate code (table 8) is applied to the data bus and this is latched into ML3 by the application of address 2F to the PA bus. Because the maximum range of the D-A output signal is approximately 0 to 10V, ML11 is powered from the +15V supply, and the +5V logic Q output signals from ML3 are level-shifted to +15V logic signals by ML4. The 16-way analogue multiplexer ML11 is permanently enabled by the '0' at the inhibit input, and the selected analogue signal is routed via the O/P pin to the metering comparator ML20a. Here it is compared with the analogue output from the D-A converter, and a software successive approximation routine then increments or decrements the binary input applied to the D-A converter until the two signals applied to the comparator are equal i.e. until the comparator output signal changes state. The binary level at the D-A converter input is then the digital equivalent of the analogue signal being measured. The D-A output signal (at TP26) is also routed to the moduation board (chap. 10) for carrier level control purposes.

Supply Metering Attenuators

13. Resistors R8 to R19 are used to provide a sample of the +12V, +15V, +20V, -15V and -30V supplies, for metering purposes. The resistor values are such that each sample is at a level of approximately 5V. Diodes D7 and D8 are included for protection purposes to clamp the -15V and -30V monitor lines to approximately -0.7V should the +15V supply fail.

Linear Amplifier Control

14. Output data strobes 24 and 25 are used to transfer linear amplifier control data from the processor data bus to rear panel connectors via two hex. D-type latches ML14, ML8, transistor inverters TR3 to TR12, and the rear panel board (tables 9 and 10). The four channel lines (table 10) are provided for the control of channelised linear amplifiers such as the Racal TA 1820. Note that a logic '1' MUTE signal from the Q4 output of ML14 is also applied to open-collector inverter TR2 to route a OV MUTE signal to the RF output amplifier board via the power supply connector.

Table 9 : Linear Amplifier Control - Strobe 24

DATA BUS	CONTROL SIGNAL	STATUS (AT REAR PANEL BOARD OUTPUT)
0	EHT ON	) OV = ON
1	STANDBY ON	) OPEN CIRCUIT = OFF
2	RESET (CTI)	NORMAL = OV, OPEN CIRCUIT = RESET
3	MUTE	NORMAL = OPEN CIRCUIT, OV = MUTE
4	TRANSMIT	OV = TRANSMIT
5	NOT USED	-

Table 10 : Linear Amplifier Control - Strobe 25

DATA BUS	CONTROL SIGNAL	STATUS (AT REAR PANEL BOARD OUTPUT)
0	POWER SELECT A	) OV = LOGIC '1'
1	POWER SELECT B	) OPEN CIRCUIT = LOGIC '0'
2	NOT USED	
3	NOT USED	
4	FSK INHIBIT	'0' = INHIBIT) TO OPTIONAL
5	FSK TEST	'0' = NORMAL) FSK BOARD

Output Data Strobe 29

15. This positive-going strobe pulse is routed via SK31 pin 4 to the synthesizer board (chap. 8) where it is used to write data into the synthesizer control stage.

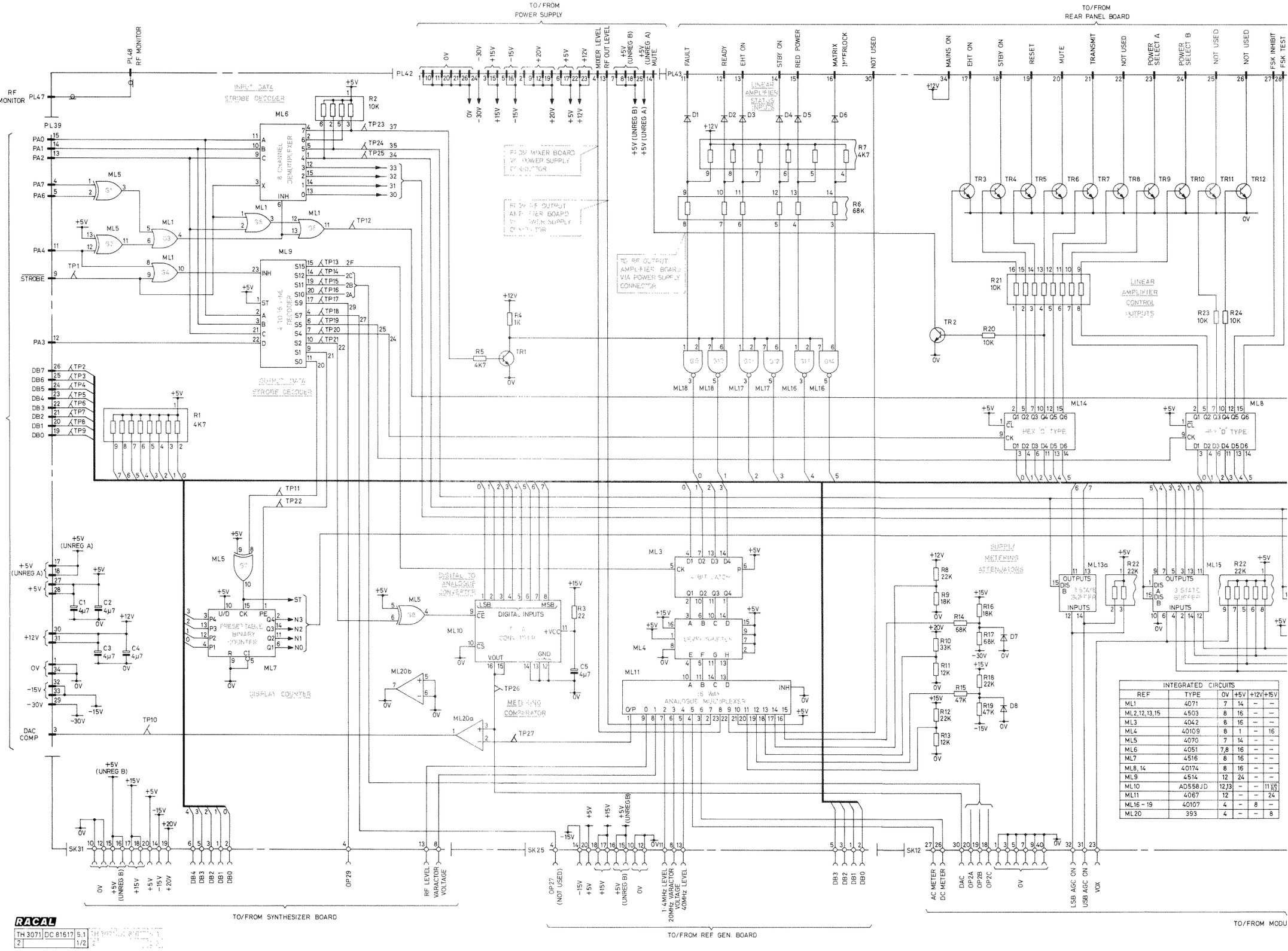
Output Data Strobes 2A, 2B and 2C

16. These three data output strobe signals are applied via SK12 pins 20, 19 and 18 to the modulation board (chap. 10) where they are used for the routeing of metering data, mode control data and audio switching control data from the processor data bus.

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
		FRONT PANEL INTERFACE BOARD (ST81617)			
Resistors					
R1	4k7	9-Resistor SIL Network			939133
R2	10k	5-Resistor SIL Network			939959
R3	22	Metal Oxide		2	920743
R4	1k	Metal Oxide		2	913489
R5	4k7	Metal Oxide		2	913490
R6	68k	8-Resistor DIL Network			939960
R7	4k7	9-Resistor SIL Network			939133
R8	22k	Metal Oxide		2	913493
R9	18k	Metal Oxide		2	900994
R10	33k	Metal Oxide		2	913495
R11	12k	Metal Oxide		2	917952
R12	22k	Metal Oxide		2	913493
R13	12k	Metal Oxide		2	917952
R14	68k	Metal Oxide		2	916478
R15	47k	Metal Oxide		2	913496
R16	18k	Metal Oxide		2	900994
R17	68k	Metal Oxide		2	916478
R18	22k	Metal Oxide		2	913493
R19	47k	Metal Oxide		2	913496
R20	10k	Metal Oxide		2	914042
R21	10k	8-Resistor DIL Network			936374
R22	22k	9-Resistor SIL Network			935012
R23	10k	Metal Oxide		2	914042
R24	10k	Metal Oxide		2	914042
R25	22k	9-Resistor SIL Network			935012
Capacitors			V		
C1	4µ7	Tantalum Bead	35	20	914026
C2	4µ7	Tantalum Bead	35	20	914026
C3	4µ7	Tantalum Bead	35	20	914026
C4	4µ7	Tantalum Bead	35	20	914026
C5	4µ7	Tantalum Bead	35	20	914026
Connectors					
PL39		Plug, 34-way			939983
PL41		Plug, 50-way			939986
PL42		Plug, 26-way			939990
PL43		Plug, 34-way			939991
PL47		Plug, coaxial			935268

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Connectors (Continued)					
PL48		Plug, coaxial			935268
SK12		Cable Assembly			BA82566/1
		Comprising:			
		PCB connector, 40-way			931768
		Socket, 40-way			934822
		Cable, flat, 40-way			931533
		Clamp, strain relief			934813
SK25		Cable Assembly			BA82564/1
		Comprising:			
		PCB connector, 20-way			939999
		Socket, 20-way			934819
		Cable, flat, 20-way			931528
		Clamp, strain relief			934810
SK31		Cable Assembly			BA82564/2
		Comprising:			
		PCB connector, 20-way			939999
		Socket, 20-way			934819
		Cable, flat, 20-way			931528
		Clamp, strain relief			934810
Diodes					
D1-D10		Silicon 1N4149			923222
Transistors					
TR1		NPN Silicon 2N2369			906842
TR2		NPN Silicon 2N2222A			923217
TR3		NPN Silicon 2N2222A			923217
TR4		NPN Silicon 2N2222A			923217
TR5		NPN Silicon 2N2222A			923217
TR6		NPN Silicon 2N2222A			923217
TR7		NPN Silicon 2N2222A			923217
TR8		NPN Silicon 2N2222A			923217
TR9		NPN Silicon 2N2222A			923217
TR10		NPN Silicon 2N2222A			923217
TR11		NPN Silicon 2N2222A			923217
TR12		NPN Silicon 2N2222A			923217
Integrated Circuits					
ML1		Quad 2-input OR gate 4071			930038
ML2		Hex Tri-state Buffer 4503			931004
ML3		Quad D-type Latch 4042			930861
ML4		Quad Level Shifter 40109			931054
ML5		Quad exclusive OR gate 4070			930856

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Intregrated Circuits (Continued)					
ML6		Single 8-Channel Demux 4051			930035
ML7		Binary up/down counter 4516			929329
ML8		Hex D-type flip-flop 40174			931060
ML9		4-line to 16-line decoder 4514			931010
ML10		8-bit D to A Converter AD558JD			939961
ML11		16-Channel MUX 4067			930998
ML12		Hex Tri-state buffer 4503			931004
ML13		Hex Tri-state buffer 4503			931004
ML14		Hex D-type flip-flop 40174			931060
ML15		Hex Tri-state buffer 4503			931004
ML16		Dual 2-input NAND buffer 40107			931052
ML17		Dual 2-input NAND buffer 40107			931052
ML18		Dual 2-input NAND buffer 40107			931052
ML19		Dual 2-input NAND buffer 40107			931052
ML20		Dual Voltage Comparator 393			939906
Miscellaneous					
		8-pin DIL IC socket			940901
		14-pin DIL IC socket			940902
		16-pin DIL IC socket			940903
		24-pin DIL IC socket			930609
		Test Point			936148



INTEGRATED CIRCUITS					
REF	TYPE	0V	+5V	+12V	+15V
ML1	4071	7	14	–	–
ML2,12,13,15	4503	8	16	–	–
ML3	4042	8	16	–	–
ML4	40109	8	1	–	16
ML5	4070	7	14	–	–
ML6	4051	7,8	16	–	–
ML7	4516	8	16	–	–
ML8, 14	40174	8	16	–	–
ML9	4514	12	24	–	–
ML10	AD558JD	12,13	–	–	11 VR3
ML11	4067	12	–	–	24
ML16 – 19	40107	4	–	8	–
ML20	393	4	–	–	8

RACAL

TH 3071	DC 81617	5.1
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TO/FROM POWER SUPPLY

TO/FROM REAR PANEL BOARD

PL42 — 0V, −30V, +15V, −15V, +20V, +5V, +12V, MIXER LEVEL, RF OUT LEVEL, +5V (UNREG B), +5V (UNREG A), MUTE

PL43 — FAULT, READY, EHT ON, STBY ON, RED POWER, MATRIX INTERLOCK, NOT USED, MAINS ON, EHT ON, STBY ON, RESET, MUTE, TRANSMIT, NOT USED, POWER SELECT A, POWER SELECT B, NOT USED, NOT USED, FSK INHIBIT, FSK TEST, −15V, 0V, EXT PTT, EXT MUTE, FSK FITTED, KEY, +12V, +15V

FROM MIXER BOARD VIA POWER SUPPLY CONNECTOR

FROM RF OUTPUT AMPLIFIER BOARD VIA POWER SUPPLY CONNECTOR

TO RF OUTPUT AMPLIFIER BOARD VIA POWER SUPPLY CONNECTOR

LINEAR AMPLIFIER STATUS INPUTS

LINEAR AMPLIFIER CONTROL OUTPUTS

D1 D2 D3 D4 D5 D6

R7 4K7

R6 68K

TR3 TR4 TR5 TR6 TR7 TR8 TR9 TR10 TR11 TR12

R21 10K

R23 10K

R24 10K

R25 22K

R4 1K

R5 4K7

TR1

TR2

R20 10K

ML18 ML18 ML17 ML17 ML16 ML16

ML14 — HEX D TYPE

ML8 — HEX D TYPE

ML13b — INPUTS, 3 STATE BUFFER, OUTPUTS

ML12b — INPUTS, 3 STATE BUFFER, OUTPUTS

R22 22K

ML13a — OUTPUTS, 3 STATE BUFFER, INPUTS

ML15 — OUTPUTS, 3 STATE BUFFER, INPUTS

ML2 — OUTPUTS, 3 STATE BUFFER, INPUTS

ML12a — OUTPUTS, 3 STATE BUFFER, INPUTS

D9 D10

PL41

PTT

ML19 ML19

PUSHBUTTON SWITCH MATRIX: ROW 7, ROW 6, ROW 5, ROW 4, ROW 3, ROW 2, ROW 1, ROW 0

DATA BUS: DB7, DB6, DB5, DB4, DB3, DB2, DB1, DB0

IP33, IP32, IP31, IP30

DISPLAY STROBE, N3, N2, N1, N0

RF SW, LINE SW

VOX SW, TX SW

+5V, +15V

LINE 2 MON., LINE 1 MON., MIC 2, MIC 1

TO/FROM FRONT PANEL DISPLAY BOARD

ML3 — 4 BIT LATCH

ML4 — LEVEL SHIFTER

ML5 — Q3

ML10 — DIGITAL INPUTS, D-A CONVERTER

DIGITAL TO ANALOGUE CONVERTER

ML11 — 16 WAY ANALOGUE MULTIPLEXER

ML20b

ML20a

METERING COMPARATOR

TP26

TP27

R3 22

C5 4µ7

SUPPLY METERING ATTENUATORS

R8 22K

R9 18K

R10 33K

R11 12K

R12 22K

R13 12K

R14 68K

R15 47K

R16 18K

R17 68K

R18 22K

R19 47K

D7 D8

INTEGRATED CIRCUITS					
REF	TYPE	0V	+5V	+12V	+15V
ML1	4071	7	14	–	–
ML2,12,13,15	4503	8	16	–	–
ML3	4042	8	16	–	–
ML4	40109	8	1	–	16
ML5	4070	7	14	–	–
ML6	4051	7,8	16	–	–
ML7	4516	8	16	–	–
ML8, 14	40174	8	16	–	–
ML9	4514	12	24	–	–
ML10	AD558JD	12,13	–	–	11 to 33
ML11	4067	12	–	–	24
ML16 – 19	40107	4	–	8	–
ML20	393	4	–	–	8

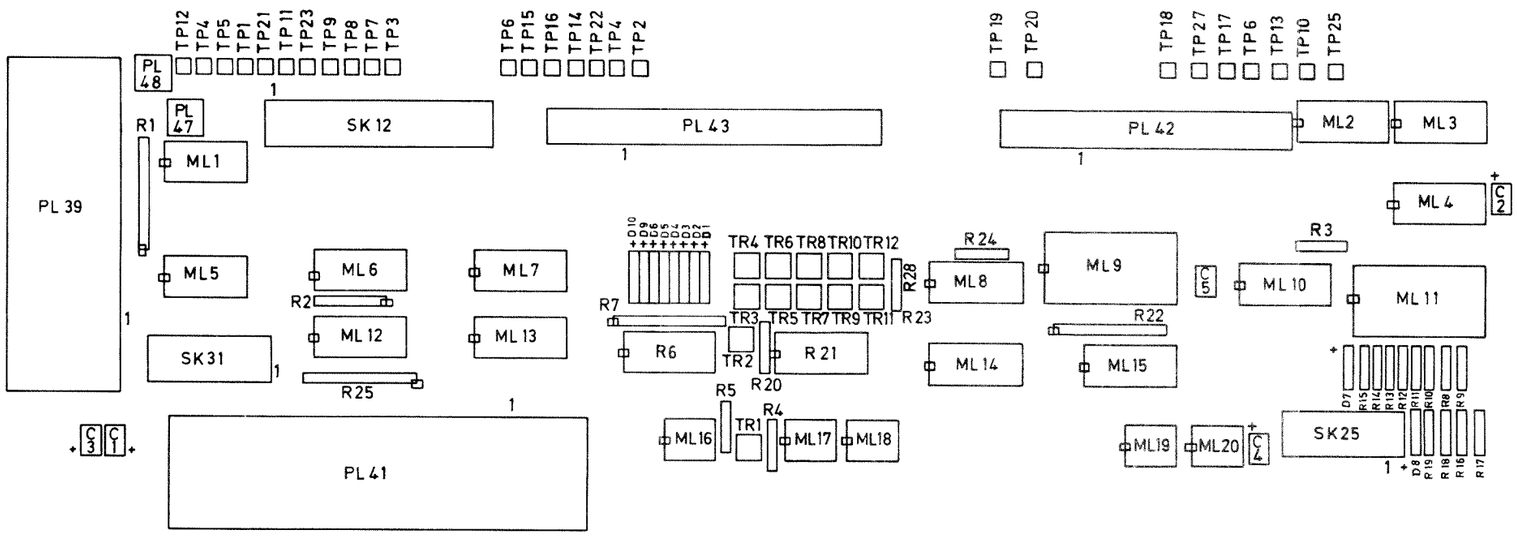
TRANSISTORS	
TR1	2N2369
TR2 – 12	2N2222A
DIODES	
D1 – 10	IN4149

TO/FROM REF GEN. BOARD: RF LEVEL, VARACTOR VOLTAGE, OP27 (NOT USED), −15V, +5V, +15V, +5V (UNREG B), 0V, 1·4MHz LEVEL, 20MHz VARACTOR VOLTAGE, 40MHz LEVEL

TO/FROM MODULATION BOARD: DB3, DB2, DB1, DB0, AC METER, DC METER, DAC, OP2A, OP2B, OP2C, 0V, LSB AGC ON, USB AGC ON, VOX, +15V, +5V, −15V, DB7, DB6, DB5, DB4, DB3, DB2, DB1, DB0, KEY, LINE 2 MON, LINE 1 MON, MIC 2, MIC 1

Circuit: Front Panel Interface Board

Fig.5.1



RACAL

TH 3071	DA 81616/4
1	

Layout: Front Panel Interface Board

Fig. 5.2

CHAPTER 6

PROCESSOR BOARD

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Tables

Illustrations

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At end of Chapter

CHAPTER 6

PROCESSOR BOARD

INTRODUCTION

1. The MA 1723 drive unit uses three devices from the 1800 microprocessor family, and all are located on the processor board. The CDP1802 C-MOS Central Processing Unit (CPU) is an 8-bit register orientated device which, in this application, uses one CDP1868 memory latch and decoder device together with an Octal D-type flip-flop type 74HC574 and a two to four line decoder type 74HC139 to interface with the memory devices (ROM, RAM and EAROM) fitted to the processor board. The remaining device of the 1800 family is a CDP1851 programmable input/output (PIO) device, which has two high-speed 8-bit I/O ports. Port A is used as a bi-directional 8-bit data bus whilst port B is used as the PA address bus, and together they form the communication link between the CPU and the remainder of the unit. The circuit diagram of the board is given in fig. 6.1 (at the end of the chapter).

CENTRAL PROCESSING UNIT

2. A simplified block diagram of the CDP1802 CPU is given in fig. 6(a). This shows the register-orientated architecture of the device and also shows all external connections; these are described in the following paragraphs.

MA0-MA7 Memory Address Bus

3. The high-order byte of a 16-bit memory address is placed on the memory address bus and is loaded into external address latches (in this application a CDP1868 memory latch and decoder device together with an Octal D-type flip-flop type 74HC574 and a two to four line decoder type 74HC139) by timing pulse TPA. The low order byte of the 16-bit memory address then appears on the memory address bus after termination of the TPA pulse.

Q Output

4. A single-bit output from the CPU which can be set or reset under program control. In this application, the Q output is used to continuously flash a light emitting diode (mounted on the processor board) whilst the program is running.

$\overline{\text{CLEAR}}$ and $\overline{\text{WAIT}}$ Inputs

5. These two control inputs allow the selection of one of four modes, as given in table 1. In this application, the $\overline{\text{WAIT}}$ input is not used (permanently connected to +5V) and this limits the operational modes to RESET and RUN according to the state of the $\overline{\text{CLEAR}}$ input.

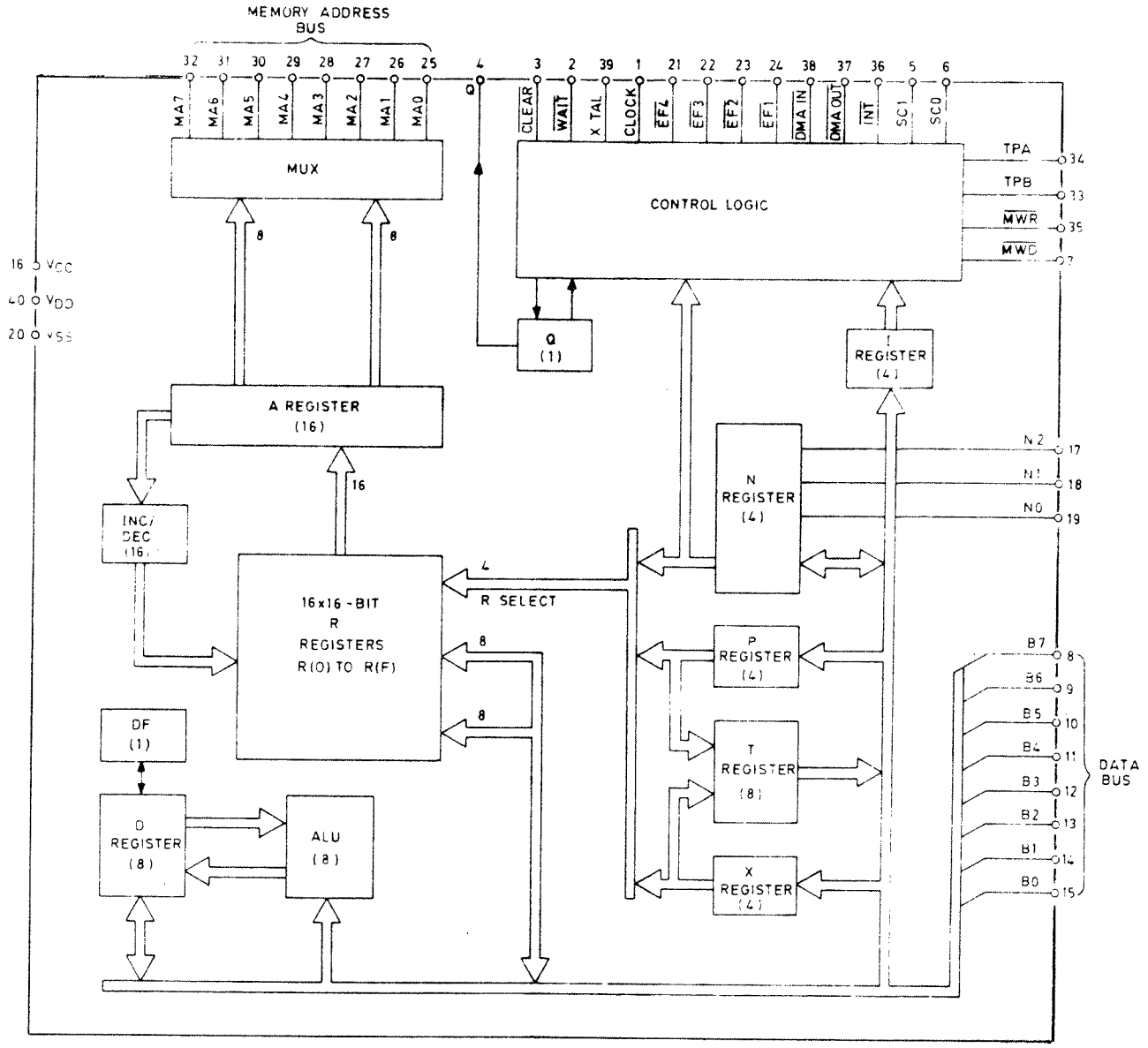


Fig. 6 (a) Simplified Block Diagram: CDP1802 CPU

Table 1 : CPU Control Modes

$\overline{\text{CLEAR}}$	$\overline{\text{WAIT}}$	MODE
0	0	LOAD
0	1	RESET
1	0	PAUSE
1	1	RUN

6. The logic level at the $\overline{\text{CLEAR}}$ input is controlled by a power on/power fail detector circuit (para. 32). This circuit is so arranged that when the unit is switched on, the RESET mode is automatically entered and is then quickly followed by the RUN mode. During the RESET mode, internal registers I, N and Q are reset, the data bus is set to the all-zero state, and interrupts are enabled. Immediately following the transition from the RESET mode to the RUN mode, an initialisation cycle commences (which clears registers R(0), X and P) and this is followed either by a DMA (direct memory access) cycle or a fetch operation from memory location 0000, dependent on the state of the $\overline{\text{DMA IN}}$ and $\overline{\text{DMA OUT}}$ inputs (para. 9).

XTAL and CLOCK Connections

7. The CPU has an internal oscillator that requires an external crystal connected between the XTAL and CLOCK pins (in this application, 2 MHz crystal XL1).

$\overline{\text{EFI}}$ to $\overline{\text{EF4}}$ Flag Inputs

8. These four flag inputs may be used to convey status information to the CPU, provided the software includes the appropriate conditional branch instructions. In this application, $\overline{\text{EFI}}$ is used to convey the setting of a board-mounted TEST switch, $\overline{\text{EF2}}$ is fed from a 16 millisecond-period squarewave output signal from a clock divider, and is used to update various software timers, $\overline{\text{EF3}}$ is used to convey the output signal from a digital-to-analogue converter (located on the front panel interface board), and $\overline{\text{EF4}}$ is unused (taken to +5V via R1).

$\overline{\text{DMA-IN}}$, $\overline{\text{DMA-OUT}}$ and $\overline{\text{INT}}$ Inputs

9. These are all interrupt request signals, where $\overline{\text{DMA-IN}}$ has the highest priority, followed by $\overline{\text{DMA-OUT}}$ and then $\overline{\text{INT}}$. The three basic ways in which the CPU can communicate with input/output (I/O) devices are (1) programmed I/O, (2) interrupt I/O and (3) direct memory access (DMA). In the programmed I/O mode, all data transfer is controlled and timed by the program. In the interrupt I/O mode, the CPU responds to an I/O generated signal. In the DMA mode, a direct high-speed data channel is established between memory and the I/O device.

10. The levels present at the $\overline{\text{DMA-IN}}$, $\overline{\text{DMA-OUT}}$ and $\overline{\text{INT}}$ inputs are sampled by the CPU during the interval between the leading edges of two timing signals TPA and TPB (para. 13). When either $\overline{\text{DMA-IN}}$ or $\overline{\text{DMA-OUT}}$ is detected, the CPU completes the execution of the current instruction. Data is then loaded into ($\overline{\text{DMA-IN}}$) or read out of ($\overline{\text{DMA-OUT}}$) memory at the address contained in register R(0). R(0) is then incremented and the process continues for as long as the $\overline{\text{DMA}}$ signal is present. In this application, $\overline{\text{DMA-IN}}$ is unused (permanently connected to +5V), whilst $\overline{\text{DMA-OUT}}$ is used to execute a test routine when signature analysis is selected (see chapter 18).

11. The $\overline{\text{INT}}$ input is produced by the optional SCORE interface board (chap. 14); it occurs every eight SCORE clock periods and also when a correct synchronisation code is detected.

SC1 and SC0 Outputs

12. The levels present at these two outputs denote the current CPU state; they are available for external gating purposes, although are not used in this application. The CPU machine cycle during which an instruction byte is fetched from memory is called state S0 (SC1 and SC0 both at '0'), whilst the cycle during which the instruction is executed is called S1 (SC0 at '1'). During the execution of a program, the CPU state generally alternates between S0 and S1. When however, a DMA request is processed, or an interrupt request is acknowledged, then the CPU state is called S2 or S3 respectively. The four CPU states are shown in table 2.

Table 2 : CPU State Coding

STATE TYPE	STATE CODE LINES SC1	SC0
S0 (FETCH)	0	0
S1 (EXECUTE)	0	1
S2 (DMA)	1	0
S3 (INTERRUPT)	1	1

TPA, TPB, $\overline{\text{MWR}}$ and $\overline{\text{MWD}}$ Timing Signals

13. Positive-going timing pulses occur at both TPA and TPB once in each machine cycle (TPB follows TPA). The state of $\overline{\text{MWR}}$ and $\overline{\text{MWD}}$ determines whether a byte is to be read from the addressed location, written into it or neither operation performed (table 3).

Table 3 : Memory Control Lines

CPU LINES	MEMORY READ	MEMORY WRITE	NON-MEMORY OPERATION
$\overline{\text{MRD}}$	0	1	1
$\overline{\text{MRW}}$	1	0	1

NO, N1 and N2 Input/Output Command Lines

14. These software-controlled outputs are used as command codes or I/O device selection codes. All three lines are at '0' except when an I/O instruction is being executed. During this time, the state of the three N bits is the same as that of the least significant three bits in the N register.

B0 to B7 Data Bus

15. This is an 8-bit bi-directional bus for the transfer of data between the CPU, memory and I/O devices.

Vcc, Vdd and Vss Supply Lines

16. The internal voltage supply Vdd is isolated from the input 1 output voltage supply Vcc so that the processor may operate at maximum speed whilst interfacing with external circuitry operating from a +5V supply (Vcc must be less than or equal to Vdd, and all outputs swing from Vss (0V) to Vcc). In this application, the Vdd and Vcc lines are connected together and are fed from a +5V supply.

MEMORY INTERFACE DEVICE CDP1868

17. One of these devices (ML13 - fig. 6.1) is used together with an Octal D-type flip-flop type 74HC574 (ML17 - fig 6.1) and a two to four line decoder type 74HC139 (ML12b - fig. 6.1) to interface the CPU with the memory devices. ML13 consists of a 4-bit latch and a decoder; a functional diagram is given in fig. 6(b) and associated truth tables are given in tables 4 and 5.

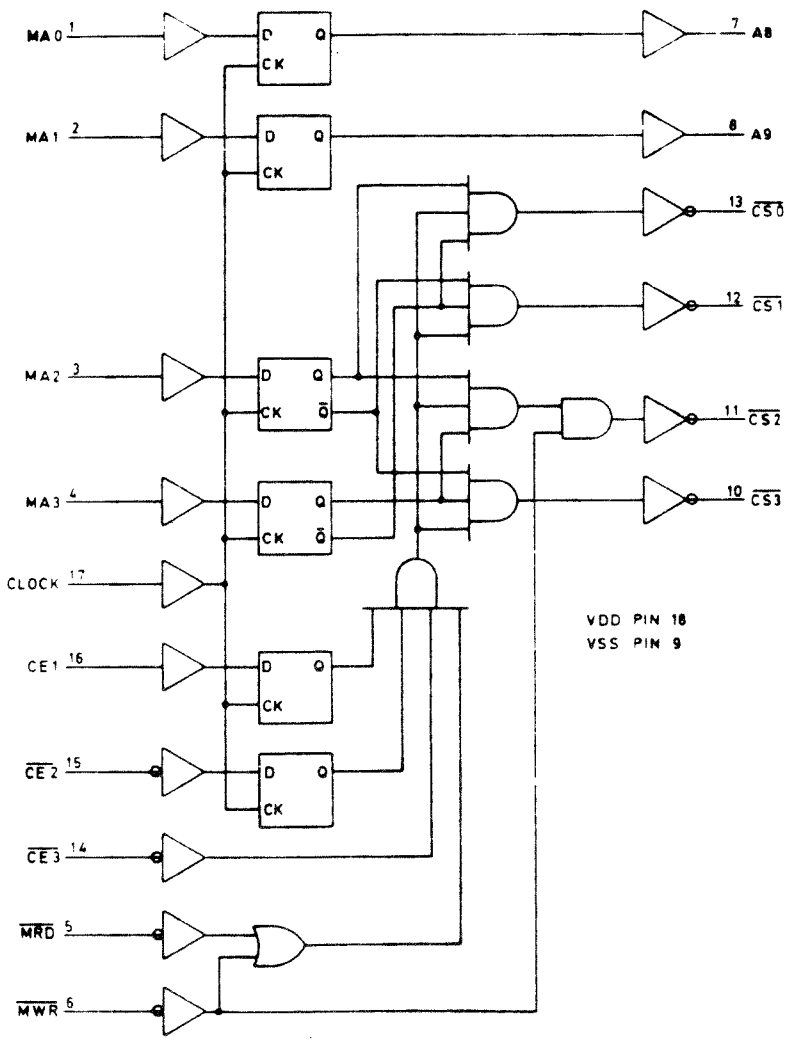


Fig.6(b) Functional Diagram: CDP1868

Table 4 : CDP1868 $\overline{CS}$ Outputs

	INPUTS								OUTPUTS			
	$\overline{MRD}$	$\overline{MWR}$	CE1	$\overline{CE2}$	$\overline{CE3}$	CK	MA3	MA2	$\overline{CS0}$	$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$
	0	0	1	0	0	1	0	0	0	1	1	1
	0	1	1	0	0	1	0	0	0	1	1	1
	1	0	1	0	0	1	0	0	0	1	1	1
	0	0	1	0	0	1	0	1	1	0	1	1
	0	1	1	0	0	1	0	1	1	0	1	1
	1	0	1	0	0	1	0	1	1	0	1	1
*	0	0	1	0	0	1	1	0	1	1	0	1
	0	1	1	0	0	1	1	0	1	1	1	1
*	1	0	1	0	0	1	1	0	1	1	0	1
	0	0	1	0	0	1	1	1	1	1	1	0
	0	1	1	0	0	1	1	1	1	1	1	0
	1	0	1	0	0	1	1	1	1	1	1	0
	1	1	X	X	X	X	X	X	1	1	1	1
	X	X	0	X	X	X	X	X	1	1	1	1
	X	X	X	1	X	X	X	X	1	1	1	1
	X	X	X	X	1	X	X	X	1	1	1	1

X Denotes either 0 or 1

* For these two conditions, $\overline{CS2}$ follows $\overline{MWR}$ regardless of the state of $\overline{MRD}$

18. The high-order byte of a 16-bit memory address from the CPU is clocked into ML13 and ML17 by the TPA clock signal, and the decoded result is latched at the chip select ($\overline{CS0}$ to $\overline{CS3}$) of ML13 and the Y0 to Y3 outputs of ML12b, for application to the addressed device. The low-order byte of the 16-bit memory address from the CPU is then applied direct to the addressed device.

Table 5 : ML12b Operation

ML12b INPUTS A15	ML12b INPUTS A14	ADDRESS RANGE	MEMORY ENABLED
0	0	0000 - 3FFF	PD1 (ROM)
0	1	4000 - 7FFF *	ML2 - ML5 (RAM EAROM)
1	0	8000 - BFFF	PD2 (ROM)
1	1	C000 - FFFF	SELF TEST SELECT SWITCHES

* This address range is decoded by ML13.

READ ONLY MEMORY

19. Provision is made for fitting two 16k by 8-bit read only memory (ROM) devices, designated PD1 and PD2, which contain the operating program and a number of test routines. PD2 is only fitted in cases where a large program is used requiring more than 16k bytes of ROM. An examination of Table 5 shows the address range applicable to the various memory types and the self test select switches.

20. The ROM devices usually fitted to the processor board are of the ultra-violet (UV) erasable type (these may be identified from all other types in that a transparent window is set into the top surface). When UV erasable type devices are in use they must at all times be protected from direct light.

ROM REPLACEMENT INSTRUCTIONS

21. Ensure that all three ROM devices fitted to the processor board have the same last suffix letter and the same program issue number. When ordering a replacement ROM device, quote the MA 1723 serial number, the B/S number (if present) of the processor board and the full information printed on the label attached to the faulty device. The label information takes the following form:

P80000/1/A
Iss. 1

where:

(1) P80000 is the system software reference number.

(2) The first suffix number (1 in this example) is the programmed device (PD) number.

(3) The second suffix (A in this example) defines the type of ROM device.

(4) Iss. denotes the program issue number (1 in this example).

RANDOM ACCESS MEMORY

22. The RAM comprises two 256 by 4-bit static C-MOS devices, ML4 and ML5. The separate data input (DI) and data output (DO) connections are joined and connected to the CPU data bus. Two chip select signals, $\overline{CS1}$ and CS2, are provided. The $\overline{CS1}$ signal, which is produced by ML13 ($\overline{CS0}$ output) and is routed by transmission gate ML14b, goes to a '0' for addresses in the range 4000 to 40FF (tables 3, 4 and 5) whilst the CS2 signal, together with the control input signal for ML14b, is fed from the $\overline{CLEAR}$ line. This line is normally at '1' and goes to '0' should the level of the +5V unregulated A supply (approximately 10V) fall below approximately 7V (para. 32).

ELECTRICALLY ALTERABLE ROM

23. ML2 and ML3 are 1K by 4-bit, non-volatile electrically alterable read only (EAROM) devices. They are used for the storage of pre-programmed channel information (channels 00 to 99), as well as the storage of front panel setting information each time a MODE button or the ENTER button is pressed, so that the unit returns to these same settings following an interruption in the supply.

24. Each EAROM device has an active-low chip-enable ($\overline{CE}$) input, an active-low write enable ($\overline{WE}$) input, and two mode control inputs, C0 and C1. The code set on the two mode control lines (table 6) is latched into the device on the negative-going edge of the $\overline{CE}$ signal.

Table 6 : EAROM Mode Control

C1	C0	Mode
0	0	READ
0	1	WRITE
1	0	BLOCK ERASE (Not Used)
1	1	WORD ERASE

25. In order to write to EAROM, the $\overline{WE}$ input must be taken low when the address and data bus lines are in a valid and static state. To achieve this, the '1' at the $\overline{MRD}$ output of the CPU is delayed by four clock cycles by shift register stage ML7a and is then inverted by ML8a to enable address decoder ML13. This allows time for the address and data bus lines to become static before either ML2 or ML3 is enabled by a '0' at the $\overline{CS2}$ or $\overline{CS3}$ output respectively of ML13. Tri-state buffer ML11a allows protection of EAROM under software control (via ML9 pin 24), and also when

signature analysis is selected by the closure of switch SB. ML8a is subsequently reset by ML7b, when $\overline{MWR}$ and $\overline{MRD}$ both return to the '1' (non-memory-operation) state.

EAROM ADDRESSING

26. The EAROM devices require that each write or erase cycle is followed by a dummy read cycle. When in the read mode, data is read during each $\overline{CE}$ pulse. Writing or erasing of a word continues for as long as the device is latched in the write or erase mode. Since the C0 and C1 mode control pins are connected to the A10 and A11 address lines, the required sequence of modes is attained under software control by the application of the appropriate addresses. The read, write and erase addresses for both ML2 and ML3 (which may be obtained by examination of tables 3, 4, 5 and 6) are given in table 7.

Table 7 : EAROM Addresses

ADDRESS									MODE	DEVICE
HEX	15	14	13	12	11	10	9	8		
6000 63FF	0 0	1 1	1 1	0 0	0 0	0 0	0 1	0 1	READ	ML2
6400 67FF	0 0	1 1	1 1	0 0	0 0	1 1	0 1	0 1	WRITE	
6C00 6FFF	0 0	1 1	1 1	0 0	1 1	1 1	0 1	0 1	WORD ERASE	
7000 73FF	0 0	1 1	1 1	1 1	0 0	0 0	0 1	0 1	READ	ML3
7400 77FF	0 0	1 1	1 1	1 1	0 0	1 1	0 1	0 1	WRITE	
7C00 7FFF	0 0	1 1	1 1	1 1	1 1	1 1	0 1	0 1	WORD ERASE	

SELF TEST SWITCHES

27. The four in-line switches, SC to SF, are for the selection of a particular test program (stored in ROM). The state of these switches is periodically checked by the CPU by the application of any address in the range C000 to FFFF. This results in a negative-going pulse at the $\overline{CS3}$ output of ML12, the disable condition is momentarily removed from tri-state buffer ML11b, and the state of the switches is conveyed to the CPU via data bus lines D0 to D3.

CDP1851 PIO DEVICE

28. ML9 (fig. 6(c)) is a programmable, two-port, input/output device, with four programmable modes, input, output, bi-directional and bit-programmable. Port A is programmable for all modes, whilst port B is programmable for the input, output and bit-programmable modes. In this application, port A is normally programmed for the output mode and is periodically briefly set to the input mode when data input is required, whilst port B is set to the bit programmable mode with all lines programmed to be outputs.

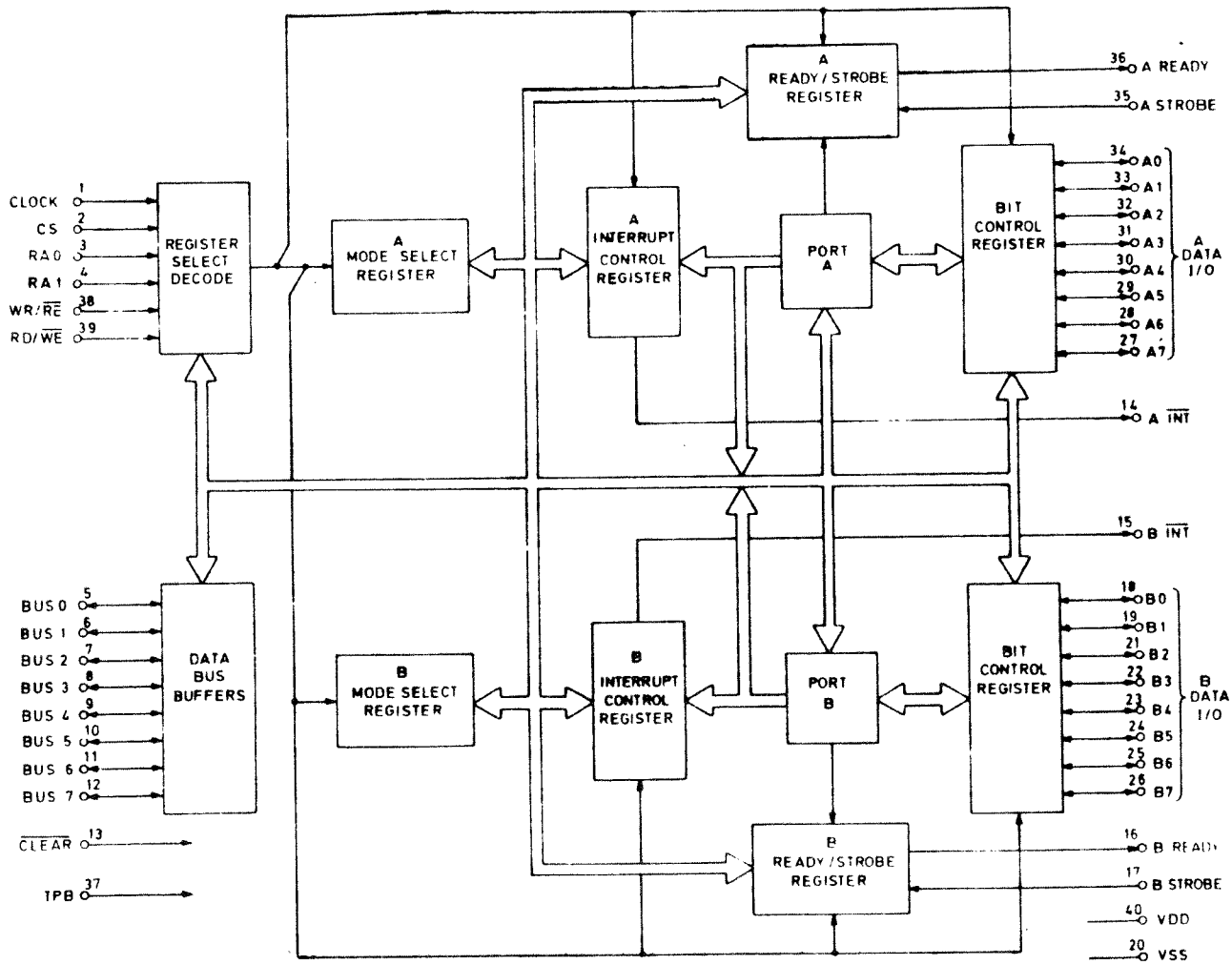


Fig.6(c) Simplified Block Diagram: CDP1851 PIO

29. The PIO device is cleared by a high-to-low transition at the $\overline{\text{CLEAR}}$ input when the unit is switched on. This resets a number of internal registers and also sets both A and B ports to the input mode. The required mode is then programmed by the application of the appropriate levels to the control inputs CS (chip select), RA0 and RA1 (register selection), WR/$\overline{\text{RE}}$ (WRITE/$\overline{\text{READ ENABLE}}$) and RD/$\overline{\text{WE}}$ (READ/$\overline{\text{WRITE ENABLE}}$), to select the control register (table 8), together with the appropriate levels at data bus lines 0 to 7 (table 9).

Table 8 : PIO Control Inputs

CS	RA1	RA0	RD/$\overline{\text{WE}}$	WR/$\overline{\text{RE}}$		ACTION
0	X	X	X	X	)	NO OPERATION. BUS IN HIGH
X	0	0	X	X	)	IMPEDANCE STATE
X	X	X	0	0	)	
X	X	X	1	1	)	
1	0	1	1	0	*	READ STATUS REGISTER
1	0	1	0	1		LOAD CONTROL REGISTER
1	1	0	1	0	*	READ PORT A
1	1	0	0	1		LOAD PORT A
1	1	1	1	0	*	READ PORT B
1	1	1	0	1		LOAD PORT B

X Denotes 0 or 1

* READ : RD/$\overline{\text{WE}}$ at '1' and WR/$\overline{\text{RE}}$ at '0' at trailing edge of CLOCK (TPA)

Table 9 : Control Register Selection

DATA BUS								ACTION
7	6	5	4	3	2	1	0	
0	0	X	B	A	X	1	1	Set Port Input Mode
0	1	X	B	A	X	1	1	Set Port Output Mode
1	0	X	0	1	X	1	1	Set A Port Bi-directional Mode
1	1	X	B	A	X	1	1	Set Port Bit-programmable Mode

A and B : 1 to Set

X : Either 0 or 1

30. Port A is used for the two-way transfer of data between the CPU and other parts of the unit on the application of the appropriate strobe pulse (generated on the front panel interface board), which is controlled by the port B output. When port A is set to the input mode, a dummy read cycle is executed to produce a '1' at the 'A' RDY output; this is applied to the D input of strobe pulse generator ML8b such that at the next positive-going transition of the TPA clock signal, the following action ensures:

(1) A '0' is produced at the $\overline{Q}$ output of ML8b; this is applied to a 4-line to 16-line decoder on the front panel interface board (chap. 5) producing a strobe pulse at one of the sixteen output pins, as selected by the levels at the PA0 to PA3 address bus lines i.e. the PIO port B lines 0 to 3.

(2) A '1' is produced at the Q output of ML8b; this is applied to the A STROBE input of ML9, and the data at the port A input line (resulting from the $\overline{\text{STROBE}}$ output produced by ML8b) is loaded into ML9 for transfer to the CPU via the data bus.

(3) ML8b is then reset by the next TPB clock pulse, the '0' at the Q output terminates the A STROBE pulse, and the '1' at the $\overline{Q}$ output inhibits the 4-line to 16-line decoder device on the front panel interface board.

31. The action of the circuit when port A is set to the output mode is similar, except that:

(1) The output data is latched at the port A output pins before a '1' occurs at the 'A' RDY output.

(2) The $\overline{\text{STROBE}}$ pulse at the $\overline{Q}$ output of ML8b is routed to an 8-channel demultiplexer on the front panel interface board to produce the appropriate input data strobe pulse.

POWER ON RESET/POWER FAIL DETECTOR

32. The purpose of this circuit is to produce the power-on $\overline{\text{CLEAR}}$ signal required by the CPU (ML1) and the PIO (ML9), and subsequently to reapply the clear signal should the +5V unregulated A supply (approximately +10V) fall below approximately +7V. It is also used to switch the -30V supply to the EAROM devices such that it is applied after application of the +5V supply and is removed before removal of the +5V supply (a protection requirement of the EAROM devices).

33. The $\overline{\text{CLEAR}}$ signal is produced by voltage comparator ML15a and inverter TR1. A precision voltage reference device ML16 sets the level at the non-inverting input of ML15a to 1.26V, whilst potential divider R8, R9 applies a sample of the +5V unregulated A supply (approximately 1.7V) to the inverting input of ML15a. At switch on, the $\overline{\text{CLEAR}}$ line is at '0' and goes to a '1' when the level at the inverting input of ML15a rises above the 1.26V reference level (C9 is included to ensure that the $\overline{\text{CLEAR}}$ line is held low for the duration of several CPU clock cycles to initialise the CPU). Should the level of the +5V unregulated A supply fall below approximately +7V, then the output of ML15a changes state, TR1 and TR2 are both turned off, the $\overline{\text{CLEAR}}$ line returns to 0V and TR3 turns off to remove the -30V supply from the EAROM devices.

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
		PROCESSOR BOARD (ST86051)			
Resistors					
R1	100k	9-Resistor SIL Network			938049
R2	100k	Metal Oxide		2	915190
R3	4k7	Metal Oxide		2	913490
R4	1M	Metal Oxide		2	918121
R5	22k	Metal Oxide		2	913493
R6	100k	Metal Oxide		2	915190
R7	2k2	Metal Oxide		2	916546
R8	10k	Metal Oxide		2	914042
R9	2k2	Metal Oxide		2	916546
R10	10k	Metal Oxide		2	914042
R11	10k	Metal Oxide		2	914042
R12	10k	Metal Oxide		2	914042
R13	4k7	Metal Oxide		2	913490
R14	10k	Metal Oxide		2	914042
R15	1k	Metal Oxide		2	913489
R16	100k	Metal Oxide		2	915190
R17	22k	Metal Oxide		2	913493
R18	22k	Metal Oxide		2	913493
R19	10k	9-Resistor SIL Network			934506
R20	10k	9-Resistor SIL Network			934506
Capacitors			V		
C1	1µ0	Tantalum Bead	35	20	923571
C2	10n	Ceramic Disc	250	+40-20	900067
C3	1µ0	Tantalum Bead	35	20	923571
C4	1µ0	Tantalum Bead	35	20	923571
C5	4µ7	Tantalum Bead	35	20	914026
C6	4µ7	Tantalum Bead	35	20	914026
C7	4µ7	Tantalum Bead	35	20	914026
C8	4µ7	Tantalum Bead	35	20	914026
C9	2µ2	Tantalum Bead	35	20	923572
Inductors					
L1	10µH	Choke		10	922364
Switches					
S1		DIL Switch bank SA, SB			932881
S2		DIL Switch bank SC to SF			933738

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Connectors					
PL40		Plug, 34-way			939991
SK39		Cable assembly			BA82563/1
		Comprising:			
		Connector PCB, 34-way			940000
		Socket, 34-way			934821
		Cable, flat, 34-way			931531
		Clamp, Strain relief			934812
Crystals					
XL1		Quartz 2 MHz			AD81793/1
Diodes					
D1		LED, Red MV5074B			931291
Transistors					
TR1		PNP Silicon 2N2906A			939909
TR2		PNP Silicon 2N2906A			939909
TR3		NPN Silicon 2N2222A			923217
Integrated Circuits					
ML1		Microprocessor CDP1802CE			939301
ML2		1K x 4-bit EAROM ER3400			934622
ML3		1K x 4-bit EAROM ER3400			934622
ML4		Static C-MOS RAM MWS5101			939180
ML5		Static C-MOS RAM MWS5101			939180
ML6		12-Stage Ripple Counter 4040			931144
ML7		Dual 4-stage shift register 4015			930973
ML8		Dual D-type flip-flop 4013			926860
ML9		Programmable I/O CDP1851CE			939181
ML10		-12V Regulator 79M12			938563
ML11		Hex Tri-state buffer 4503			931004
ML12		Memory Address Latch 74HC139			943068
ML13		Memory Address Latch CDP1868CE			939182
ML14		Quad Transmission gate 4066			930148
ML15		Dual Voltage Comparator 393			939906
ML16		Precision Voltage Reference ZN423T			939905
ML17		Octal D-type flip flop 74HC574			943069
PD1		)Programmed ROM			
PD2		)Devices - see text			

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Miscellaneous					
		Test Point			936148
		Captive Fastener			930396
		8-pin DIL IC socket			940901
		14-pin DIL IC socket			940902
		16-pin DIL IC socket			940903
		18-pin DIL IC socket			940904
		22-pin DIL IC socket			930608
		24-pin DIL IC socket			930609
		40-pin DIL IC socket			930613
		28-pin DIL IC socket			930610

PL40

+12V

+5V

0V

-12V

INTERRUPT

SCOPE INTERNAL CLOCK

ML7a

ML7b

ML8a

MRD DELAYED BY 4 CLOCK CYCLES

ADDRESS VALID TIMING

SHIFT REGISTER

R5 22K

ML14a

USED AS AND GATE

ADDRESS VALID

TP3

ML13

ALL ADDRESS LINES STATIC

ADDRESS LATCH AND DECODER

ML17

ML12b

ML14b

R16 100K

TP4

SIGNATURE ANALYSIS START / STOP

R1 100K

R3 4K7

D1

TP8

RUN/FAULT INDICATOR

XL1 2MHz

R4 1M

ML1

CPU

DMA OUT

EF1

INT EF4 EF2 EF3 N2 N1 N0 B7 B6 B5 B4 B3 B2 B1 B0

TPA

TPB

CLEAR

SA TEST

SB SIG ANALYSIS

ML6

TP9

R2 100K

TP2

TP1

CLOCK DIVIDER

SIGNATURE ANALYSIS CLOCK

ADDRESS 0000-3FFF

ADDRESS 8000-BFFF

PD1

PD2

ML4

256X 4-BIT RAM ADDRESS 4000 - 40FF

R6 100K

TP6

ML9

PROGRAMMABLE I/O INTERFACE

DATA BUS

PORT A

PORT 'B'

'B' STROBE

A STROBE

'A' RDY

WR/RE

RD/WE

ML8b

STROBE GENERATOR

STROBE

DAC COMP

SK39

R7 2K2

R8 10K

ML15a

R10 10K

R11 10K

TR1

R13 4K7

R9 2K2

C1 1µ0

C9 2µ2

ML16

+Ve VOLTAGE REFERENCE -Ve

POWER ON RESET / POWER FAIL DETECTOR

TR2

R12 10K

TP7

-30V

TR3

R14 10K

R15 1K

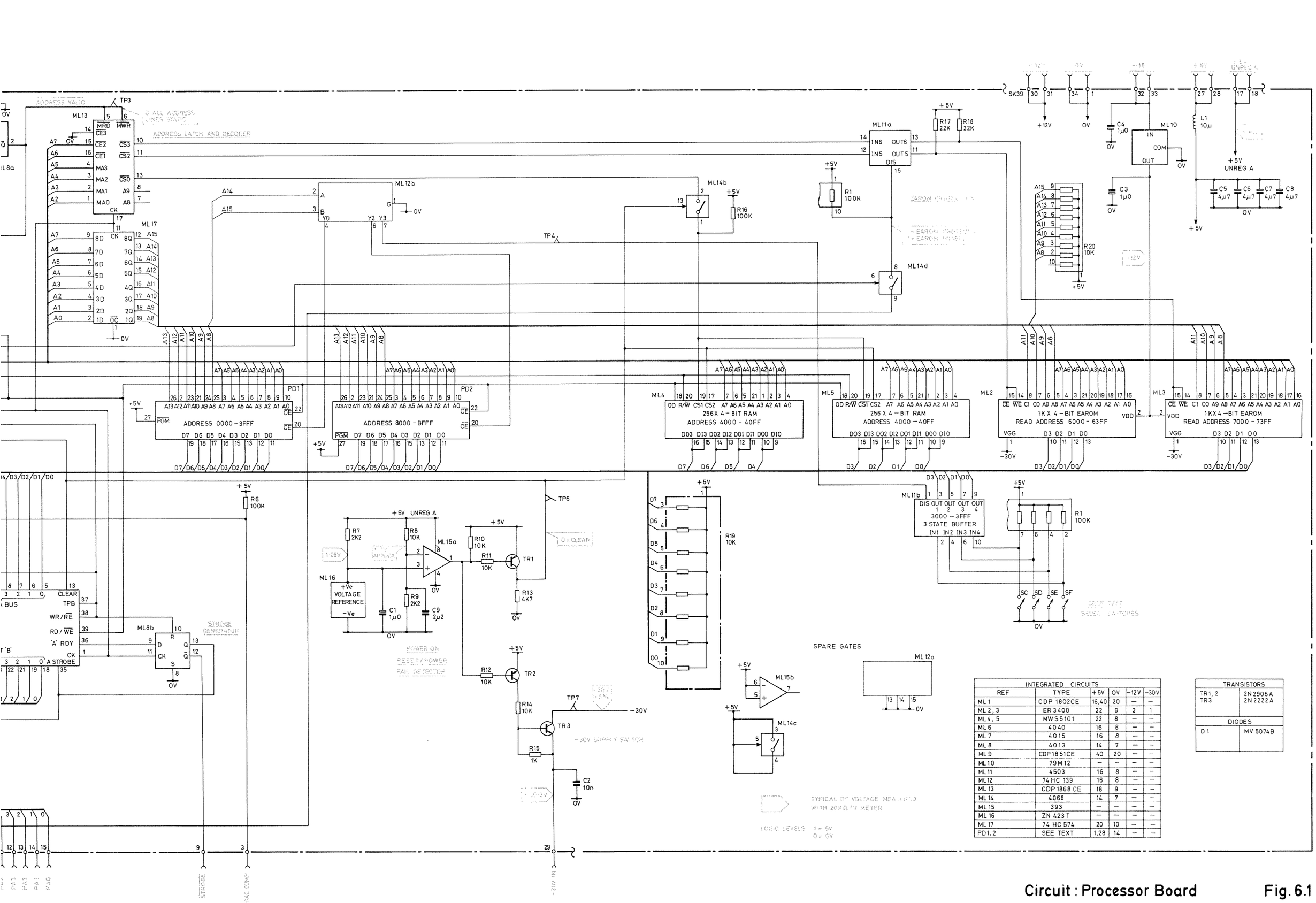
C2 10n

R19 10K

ML15b

ML14c

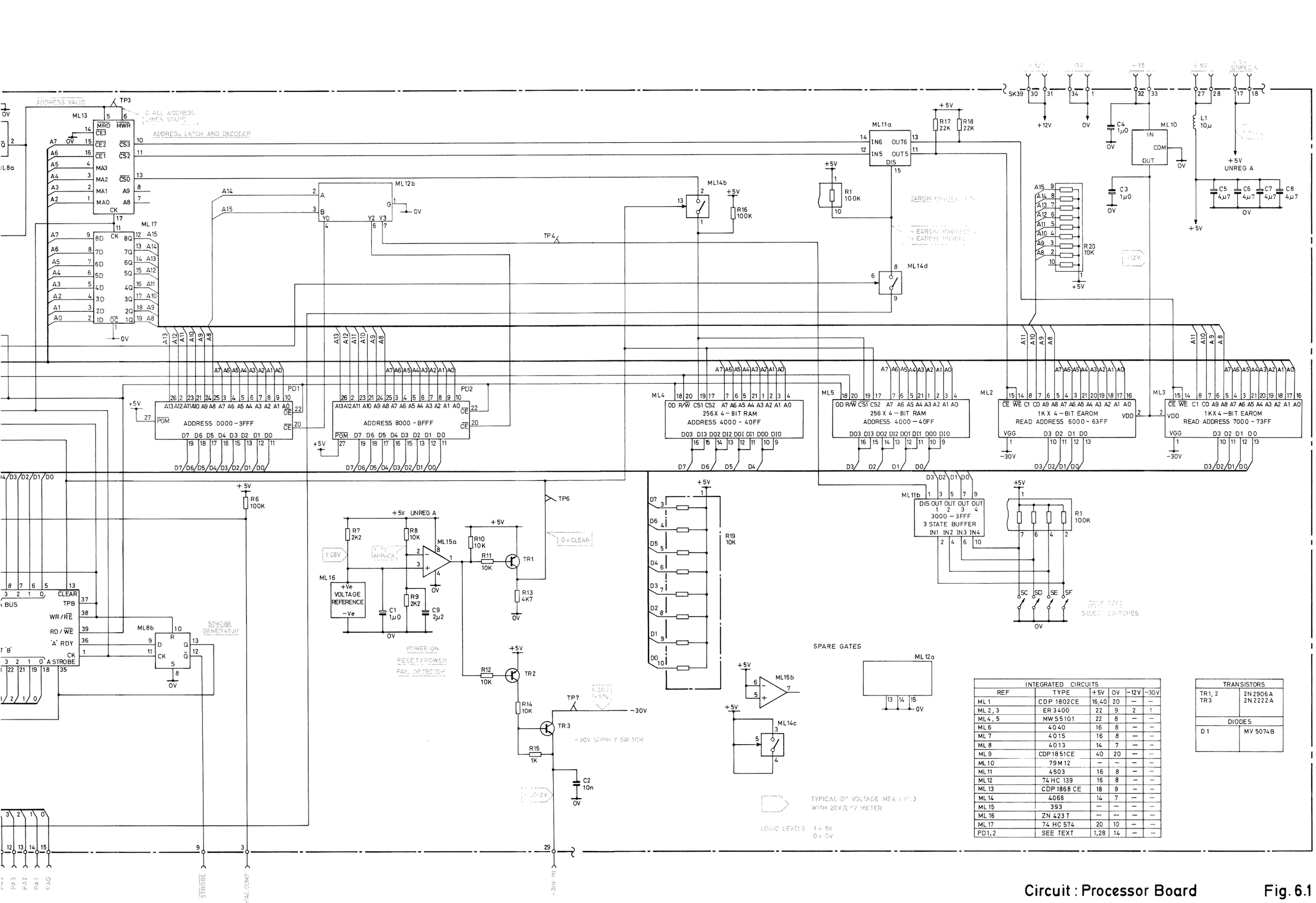
LOGIC LEVELS



INTEGRATED CIRCUITS					
REF	TYPE	+5V	0V	-12V	-30V
ML 1	CDP 1802CE	16,40	20	—	—
ML 2, 3	ER 3400	22	9	2	1
ML 4, 5	MWS 5101	22	8	—	—
ML 6	4040	16	8	—	—
ML 7	4015	16	8	—	—
ML 8	4013	14	7	—	—
ML 9	CDP 1851CE	40	20	—	—
ML 10	79M12	—	—	—	—
ML 11	4503	16	8	—	—
ML 12	74 HC 139	16	8	—	—
ML 13	CDP 1868 CE	18	9	—	—
ML 14	4066	14	7	—	—
ML 15	393	—	—	—	—
ML 16	ZN 423 T	—	—	—	—
ML 17	74 HC 574	20	10	—	—
PD1, 2	SEE TEXT	1,28	14	—	—

TRANSISTORS	
TR1, 2 TR3	2N 2906 A 2N 2222 A
DIODES	
D 1	MV 5074 B

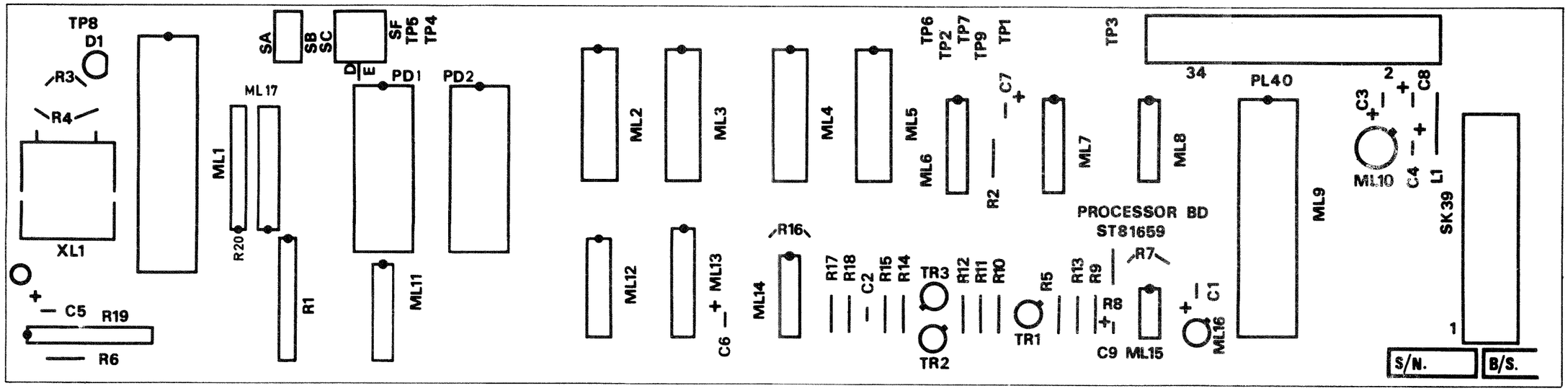
Circuit : Processor Board **Fig. 6.1**



INTEGRATED CIRCUITS					
REF	TYPE	+5V	0V	-12V	-30V
ML 1	CDP 1802CE	16,40	20	—	—
ML 2, 3	ER 3400	22	9	2	1
ML 4, 5	MWS 5101	22	8	—	—
ML 6	4040	16	8	—	—
ML 7	4015	16	8	—	—
ML 8	4013	14	7	—	—
ML 9	CDP 1851CE	40	20	—	—
ML 10	79M12	—	—	—	—
ML 11	4503	16	8	—	—
ML 12	74 HC 139	16	8	—	—
ML 13	CDP 1868 CE	18	9	—	—
ML 14	4066	14	7	—	—
ML 15	393	—	—	—	—
ML 16	ZN 423 T	—	—	—	—
ML 17	74 HC 574	20	10	—	—
PD1, 2	SEE TEXT	1,28	14	—	—

TRANSISTORS	
TR1, 2 TR3	2N 2906 A 2N 2222 A
DIODES	
D 1	MV 5074 B

Circuit : Processor Board **Fig. 6.1**



RACAL
TH3071 | DA 86050
1

Layout : Processor Board Fig. 6-2

CHAPTER 7

REFERENCE GENERATOR BOARD

CONTENTS

Tables

Illustrations

Text

At end of Chapter — Fig.

CHAPTER 7

REFERENCE GENERATOR BOARD

INTRODUCTION

1. This board accepts a reference frequency input signal from either an internal or externally connected frequency standard, and produces output signals at 1.4 MHz, 20 MHz and 40 MHz. An automatic switching circuit isolates the signal from the internal standard (if fitted) when an external standard is connected to the unit.

CIRCUIT DESCRIPTION (fig. 7.1)

EXTERNAL REFERENCE INTERFACE

2. The output signal from an external frequency standard, connected to the REF IN socket SK3 on the rear panel, may be any sub-harmonic of 20 MHz between 100 kHz and 10 MHz e.g. 200 kHz, 400 kHz, 500 kHz etc. It is coupled by transformer T1 to a wideband amplifier/limiter circuit which uses three sections of a quad line receiver ML4b, ML4c and ML4d. This is an ECL (emitter coupled logic) device and contains a Vbb supply generator which is used to set the input and output threshold levels (table 1).

EXTERNAL REFERENCE DETECTOR

3. The remaining section of ML4 (ML4a) is used as an external reference detector circuit. When an external reference signal is present, the positive-going edges of the output signal from Schmitt trigger ML4c are applied via C2 to the non-inverting input of ML4a; the resulting positive output from ML4a holds C5 in a charged state, and also results in the following:

   (1) A high level at the output of voltage comparator ML1a to gate the external reference signal to the phase comparator.

   (2) A low level at the outputs of both ML1b and ML1c to effectively switch off the internal reference interface ML3.

4. When an external reference is not connected to the unit, the output from ML4a falls to approximately OV, C5 is discharged, and the output signals from voltage comparators ML1a, ML1b and ML1c assume the opposite states, as follows:

   (1) The low level at the output of ML1a causes a low level at the output of ML4d and effectively isolates the external reference interface from the phase comparator stage.

   (2) The high levels at the outputs of both ML1b and ML1c enable the internal reference interface, and the reference output from ML3d is applied to the phase comparator.

Table 1 : Quad Line Receiver Truth Table

NON-INVERTING INPUT	INVERTING INPUT	OUTPUT
L	H	L
H	L	H
L	Vbb	L
H	Vbb	H
Vbb	H	L
Vbb	L	H

INTERNAL REFERENCE INTERFACE

5. This wideband amplifier limiter stage uses three sections of ECL quad line receiver ML3b, ML3c and ML3d. The internal reference signal is coupled by C6 to the input stage ML3b and the squarewave output signal is taken from limiter stage ML3d.

20 MHz OSCILLATOR

6. TR4 is connected as a 20 MHz voltage controlled crystal oscillator. The varactor diode D3 is in series with the 20 MHz crystal XL1, and is used to shift the phase of the oscillator signal until it becomes locked to the phase of the signal derived from the frequency standard. An increase in the varactor voltage causes a decrease in capacitance and hence an increase in oscillator frequency (and vice-versa). The 20 MHz output signal is coupled by C35 to buffer stage ML8c and is then routed to:

(1) A 20 MHz output amplifier stage ML8e.

(2) A frequency doubler stage via buffer amplifier ML8d (para. 12).

(3) A 90^{o} phase shifter ML6d (para. 7).

(4) A fast lock circuit ML5b (para. 11).

(5) A phase comparator ML2b (para. 9).

(6) A 1.4 MHz generator circuit (para. 13).

QUADRATURE CORRELATOR

7. The 20 MHz output signal from ML8c is applied to the phase-shifting stage ML6d, R38, C24, which introduces a phase difference of approximately 90 degrees (fig. 7(a), waveforms 1 and 2). Provided the positive-going edge of the signal derived from the frequency standard occurs during the positive excursion of the 20 MHz quadrature signal i.e. the phase lock window, then the Q2 output of ML5a is maintained at a '1', the $\overline{Q2}$ output is maintained at a '0', TR1 and TR2 are held off, and the phase detector stage ML2a, ML2b, is effectively enabled.

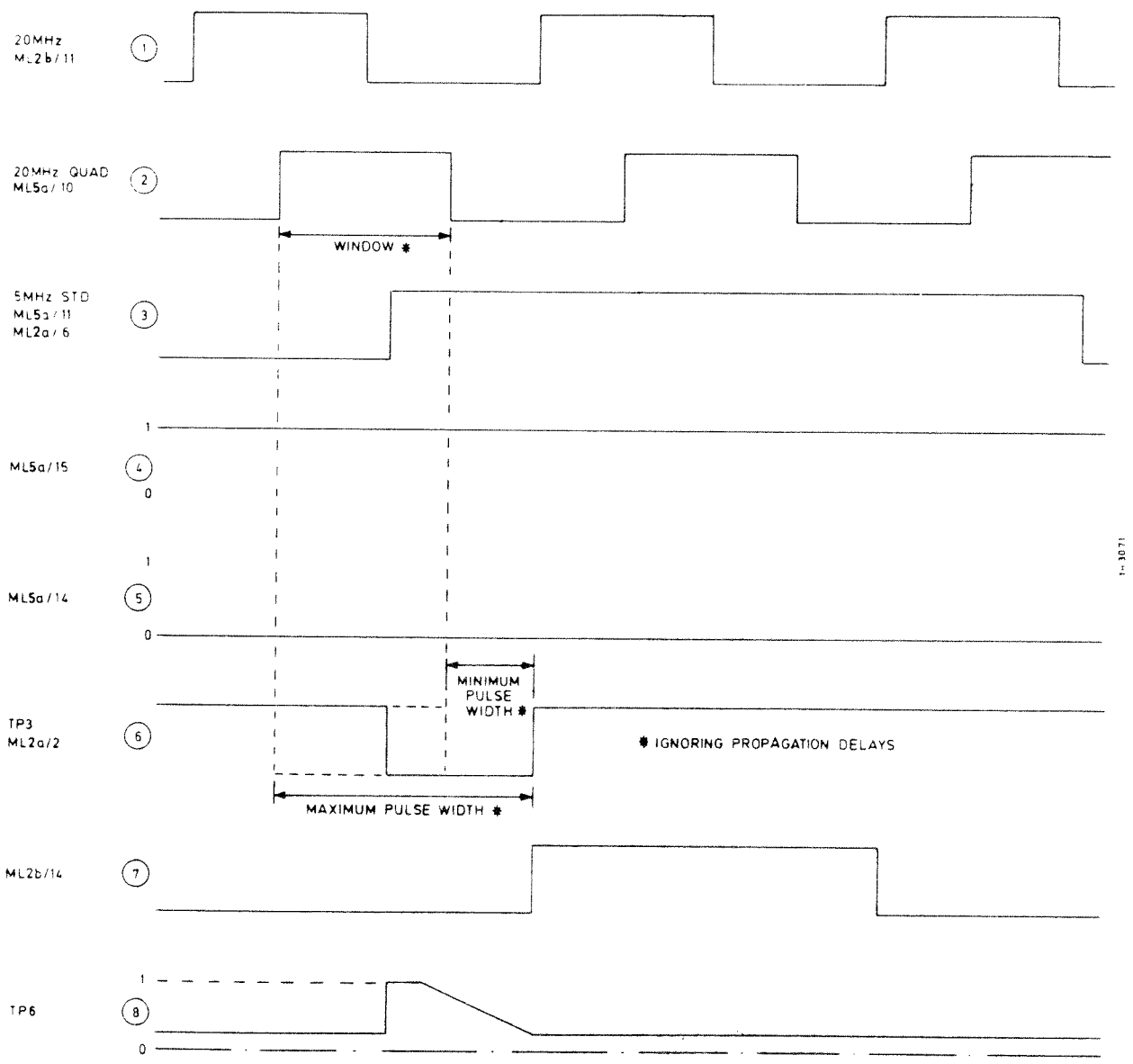


Fig.7(a) Timing Diagram: In-Lock with 5MHz Standard

8. If the positive-going edge of the signal derived from the frequency standard occurs outside the phase-lock window, then the fast-lock circuit is brought into operation and the phase detector is effectively inhibited.

PHASE COMPARATOR

9. Provided the $\overline{Q2}$ output from ML5a is at '0', then the 20 MHz signal from ML8c is applied to the clock input (CK2) of D-type flip-flop ML2b, to sample the signal derived from the frequency standard. This results in a negative-going pulse at TP3 for every positive-going transition of the frequency standard signal, where the duration of the pulse is proportional to the phase differences between the two signals.

SAMPLE AND HOLD STAGE

10. This stage (ML6c) stores a voltage in C21, the amplitude of which is proportional to the length of the pulse at TP3. When the level at TP3 goes low, the output from ML6c goes high for a short period (determined by C19, R28, R29 and R31) to charge C21. This capacitor then discharges via D2 and R32 until the level at TP3 goes high again (fig. 7(a), waveform 8). The voltage held in C21 is then applied to integrator R34, C27, ML7 to produce the varactor voltage.

FAST LOCK CIRCUIT

11. If the 20 MHz VCO frequency is either too high or too low for the lock-range of the phase comparator, i.e. the rising edge of the signal derived from the frequency standard occurs outside the phase-lock window (fig. 7(a), waveform 2), then a '1' is clocked through to the $\overline{Q2}$ output of ML5a, with the following results:

(1) A '1' is applied to the D1 input of ML2a, and this prevents the generation of the negative-going sampling pulse at TP3 i.e. the phase comparator is effectively inhibited.

(2) The '1' from the $\overline{Q2}$ output of ML5a clocks ML5b, and the level present at the D1 input ('0' for a high oscillator frequency, '1' for a low oscillator frequency) is transferred to the $\overline{Q1}$ output to switch on the appropriate fast-lock transistor, as follows:

(a) If the 20 MHz oscillator frequency is too high, the '0' at the D1 input of ML5b results in a '1' at the $\overline{Q1}$ output. Since, for this condition, the Q2 output of ML5a is at a '0', TR2 is turned on, current is fed into the (inverting) integrator, and the varactor voltage is reduced. This causes an increase in the varactor diode capacitance and hence a reduction in the oscillator frequency.

(b) If the 20 MHz oscillator frequency is too low, the '1' at the D1 input of ML5b results in a '0' at the $\overline{Q1}$ output. This time TR1 is turned on, current is drawn from the integrator, the varactor voltage level is increased, and this results in an increase in the oscillator frequency.

40 MHz OUTPUT SIGNAL

12. The 20 MHz output signal from ML8c is applied via buffer stage ML8d and common-base Q-multiplier stage TR5 to a double tuned transformer circuit, where T3, C44 and T4, C51, C52 are tuned to 40 MHz. The level detector stage ML10 is fed via Schottky diode D6 and provides a DC output voltage proportional to the level of the 40 MHz output signal. The level detector output signal is routed to the front panel interface board where it is made available to the processor for test purposes.

1.4 MHz OUTPUT SIGNAL

13. The 20 MHz output signal from ML8c is applied via buffer stage ML6b to an ECL to TTL interface stage TR3. This is fed to a divide-by-100 stage, comprising cascaded decade dividers ML13, ML12, and the resulting 200 kHz output is applied to a 1.4 MHz crystal filter. This selects the seventh harmonic of the 200 kHz input, and amplifier stage TR6, TR7 produces a 1.4 MHz output signal at a nominal level of 800 millivolts peak-to-peak. The
1.4 MHz level detector stage ML11 produces a DC output voltage proportional to the level of the 1.4 MHz output signal. This is routed to the front panel interface board for application to the processor board for test purposes.

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
		REFERENCE GENERATOR BOARD (ST81647)			
Resistors					
R1	10k	Metal Oxide		2	914042
R2	5600	Metal Oxide		2	917061
R3	180	Metal Oxide		2	915465
R4	470	Metal Oxide		2	920758
R5	470	Metal Oxide		2	920758
R6	2k2	Metal Oxide		2	916546
R7	100k	Metal Oxide		2	915190
R8	4k7	Metal Oxide		2	913490
R9	470	4-Resistor SIL Network		2	939302
R10	470	Metal Oxide		2	920758
R11	2k2	Metal Oxide		2	916546
R12	2k2	Metal Oxide		2	916546
R13	470	Metal Oxide		2	920758
R14	2k2	Metal Oxide		2	916546
R15	100	Metal Oxide		2	910388
R16	470	Metal Oxide		2	920758
R17	100	Metal Oxide		2	910388
R18	4k7	Metal Oxide		2	913490
R19	680	Metal Oxide		2	910113
R20	470	4-Resistor SIL Network		2	939302
R21	470	Metal Oxide		2	920758
R22	220	Metal Oxide		2	910390
R23	470	Metal Oxide		2	920758
R24	4k7	Metal Oxide		2	913490
R25	100	Metal Oxide		2	910388
R26	220	Metal Oxide		2	910390
R27	220	Metal Oxide		2	910390
R28	1k5	Metal Oxide		2	911166
R29	220	Metal Oxide		2	910390
R30	10k	Metal Oxide		2	914042
R31	470	Metal Oxide		2	920758
R32	470	Metal Oxide		2	920758
R33	100	Metal Oxide		2	910388
R34	270k	Metal Oxide		2	923598
R35	10	Metal Oxide		2	920736

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Resistors (Continued)					
R36	22k	Metal Oxide		2	913493
R37	47k	Metal Oxide		2	913496
R38	220	Metal Oxide		2	910390
R39	10k	Metal Oxide		2	914042
R40	10k	Metal Oxide		2	914042
R41	10	Metal Oxide		2	920736
R42	10k	Metal Oxide		2	914042
R43	680	Metal Oxide		2	910113
R44	47k	Metal Oxide		2	913496
R45	100	Metal Oxide		2	910388
R46	680	Metal Oxide		2	910113
R47	10k	Metal Oxide		2	914042
R48	10k	Metal Oxide		2	914042
R49	2k2	Metal Oxide		2	916546
R50	220	Metal Oxide		2	910390
R51	3k3	Metal Oxide		2	910111
R52	220	Metal Oxide		2	910390
R53	330	Metal Oxide		2	915690
R54	100	Metal Oxide		2	910388
R55	470	Metal Oxide		2	920758
R56	10k	Metal Oxide		2	914042
R57	100	Metal Oxide		2	910388
R58	820	Metal Oxide		2	917065
R59	47	Metal Oxide		2	917063
R60	470	Metal Oxide		2	920758
R61	15k	Metal Oxide		2	920645
R62	4k7	Metal Oxide		2	913490
Capacitors			V		
C1	1µ0	Tantalum Bead	35	20	923571
C2	10n	Ceramic Disc	250	+40-20	900067
C3	0µ1	Polycarbonate	100	10	931130
C4	1µ0	Tantalum Bead	35	20	923571
C5	1n	Ceramic Bead	500	20	915243
C6	1n	Ceramic Disc	500	20	915243
C7	10n	Ceramic Disc	250	+40-20	900067
C8	1n	Ceramic Disc	500	20	915243
C9	1n	Ceramic Disc	500	20	915243
C10	1n	Ceramic Disc	500	20	915243

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Capacitors (Continued)					
C11	1n	Ceramic Disc	500	20	915243
C12	1n	Ceramic Disc	500	20	915243
C13	10n	Ceramic Disc	250	+40-20	900067
C14	1n	Ceramic Disc	500	20	915243
C15	10n	Ceramic Disc	250	+40-20	900067
C16	10n	Ceramic Disc	250	+40-20	900067
C17	10n	Ceramic Disc	250	+40-20	900067
C18	1n	Ceramic Disc	500	20	915243
C19	100p	Ceramic Disc	500	10	917417
C20	10n	Ceramic Disc	250	+40-20	900067
C21	220p	Ceramic Disc	500	10	931148
C22	4µ7	Tantalum Bead	35	20	914026
C23	0µ1	Polycarbonate	100	10	931130
C24	68p	Ceramic Disc	500	10	917737
C25	0µ1	Polycarbonate	100	10	931130
C26	1µ0	Polycarbonate	100	10	931133
C27	47n	Polycarbonate	250	10	935141
C28	10n	Ceramic Disc	250	+40-20	900067
C29	10n	Ceramic Disc	250	+40-20	900067
C30	10n	Ceramic Disc	250	+40-20	900067
C31	1n	Ceramic Disc	500	20	915243
C32	330p	Ceramic Disc	100	5	940248
C33	100p	Ceramic Disc	100	5	940249
C34	68p	Ceramic Disc	500	10	917737
C35	10n	Ceramic Disc	250	+40-20	900067
C36	10n	Ceramic Disc	250	+40-20	900067
C37	100p	Ceramic Disc	500	10	917417
C38	68p	Ceramic Disc	500	10	917737
C39	100p	Ceramic Disc	500	10	917417
C40	10n	Ceramic Disc	250	+40-20	900067
C41	10n	Ceramic Disc	250	+40-20	900067
C42	1n	Ceramic Disc	500	20	915243
C43	1n	Ceramic Disc	100	10	939918
C44	33p	Ceramic Disc	100	5	940096
C45	1n	Ceramic Disc	500	20	915243
C46	10n	Ceramic Disc	250	+40-20	900067
C47	100p	Ceramic Disc	500	10	917417
C48	10p	Ceramic Disc	500	5	921270
C49	10p	Ceramic Disc	500	5	921270
C50	100p	Ceramic Disc	500	10	917417

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Capacitors (Continued)					
C51	33p	Ceramic Plate	100	5	940096
C52	680p	Ceramic Plate	100	5	940095
Inductors					
L1	10µH	Choke		10	922364
L2	10µH	Choke		10	922364
L3	6µ8H	Choke		10	939694
L4	6µ8H	Choke		10	939694
L5	10µH	Choke		10	922364
L6	10µH	Choke		10	922364
L7	1µH	Choke		10	938966
L8	1mH	Choke		10	926988
Transformers					
T1		Transformer assembly			AT82411
T2		Transformer assembly			AT82409
T3		Transformer assembly			AT82410
T4		Transformer assembly			AT82410
Connectors					
PL25		Plug, 20-way			939969
PL26		Plug, coaxial			935268
PL27		Plug, coaxial			935268
PL28		Plug, coaxial			935268
PL29		Plug, coaxial			935268
PL30		Plug, coaxial			935268
Crystals					
XL1		Quartz 20 MHz			AD80547
XL2		Quartz 1.399900 MHz			AD75885
XL3		Quartz 1.399900 MHz			AD75885
Diodes					
D1		Schottky 5082-2811			919460
D2		Schottky 5082-2811			919460
D3		Varactor ZC706			920266
D4		Zener, 12V, 400 mW, BZX79C12V			928372
D5		Schottky 5082-2811			919460
D6		Schottky 5082-2811			919460

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Transistors					
TR1		NPN Silicon 2N2369			906842
TR2		PNP Silicon BFX48			915231
TR3		NPN Silicon 2N2369			906842
TR4		NPN Silicon 2N2369			906842
TR5		NPN Silicon BC109			923234
TR6		NPN Silicon BC109			923234
TR7		NPN Silicon BC109			923234
Integrated Circuits					
ML1		Quad Comparator LM339N			925952
ML2		ECL Dual D-tpe flip-flop 10231P			938877
ML3		ECL Quad line receiver 10115P			938874
ML4		ECL Quad line receiver 10115P			938874
ML5		ECL Dual D-type flip-flop 10231P			938877
ML6		ECL Quad line receiver 10115P			938875
ML7		Operational Amplifier CA3140E			932204
ML8		ECL Quad line receiver 10115P			938874
ML9		5V Regulator LM340T50			939921
ML10		Operational Amplifier CA3140E			932204
ML11		Operational Amplifier CA3140E			932204
ML12		TTL Decade Counter SN74LS90N			935560
ML13		TTL Decade Counter SN74LS90N			935560
Miscellaneous					
		Test Point			936148
		Captive Fastener			930396
		8-pin DIL IC socket			940901
		14-pin DIL IC socket			940902
		16-pin DIL IC socket			940903
		Heatsink (for ML9)			933369

EXTERNAL REFERENCE INTERFACE

EXT. REF CONNECTED ≥500mV R.M.S.

PL28

T1

R3 180

R4 470

ML4b

R6 2K2

R5 470

ML4c

R8 4K7

ML4d

R12 2K2

R13 470

L1 10µ

C13 10n

ML4 1,16 Vbb

Vbb SUPPLY TO ECL LINE RECEIVERS

C11 1n

C3 0µ1

R10 470

≤0·7V NO EXT REF
3·9V WITH EXT REF

C2 10n

R2 560

ML4a

R1 10K

EXTERNAL REFERENCE DETECTOR

C5 1n

ML1a

C7 10n

C10 1n

ML1b

ML1c

R7 100K

SPARE

ML1d

INTERNAL REFERENCE INTERFACE

3·9V NO EXT REF
≤0·7V WITH EXT REF

PL27

C6 1n

ML3b

R9 470

R11 2K2

C9 1n

ML3c

R14 2K2

ML3d

L2 10µ

C15 10n

ML3 1,16 Vbb

Vbb SUPPLY TO ECL LINE RECEIVERS

C8 1n

C12 1n

C14 1n

ML3a

PL25

ML9 IN OUT COM

+15V

+5V

C1 1µ0

C4 1µ0

OV

20MHz ECL 90° LAG WITH RESPECT TO TP8

TP1

R15 100

REFERENCE FREQUENCY (FR) ECL

QUADRATURE CORRELATOR

TP2

R17 100

L3 6µ8

C16 10n

ML5a

R16 470

R18 4K7

ML5b

L4 6µ8

C17 10n

ML2a

ML2b

R20 470

FAST LOCK

TR1

TR2

TP4

R30 10K

20MHz ECL

30ns

FR

PHASE COMPARATOR

R19 680

R23 470

90° PHASE SHIFTER

TP8

R45 100

R38 220

C24 68p

ML6d

ML8a

ML6a

L5 10µ

ML6 1,16 Vbb

C28 10n

L6 10µ

ML8 1,16 Vbb

C30 10n

R43 330

ML8c

R46 680

3·9V

Vbb SUPPLY TO ECL LINE RECEIVERS

R37 47K

C26 1µ0

C27 47n

3 TO 9V

ML6c

D1

D2

TP6

R33 100

R36 22K

R34 270K

R25 100

TP3

R29 220

ML7

TP7

R42 10K

R44 47K

R39 10K

R40 10K

C29 10n

XL1 20MHz

D3

R47 10K

C19 100p

R28 1K5

R31 470

R32 470

C21 220p

C22 4µ7

SAMPLE AND HOLD

INTEGRATOR

LOOP FILTER

20MHz

R26 220

R24 2K2

R27 220

C20 10n

TR3

TP5

20MHz TTL

ML6b

R22 220

C18 1n

R21 470

ECL / TTL INTERFACE

ML13 DECADE DIVIDER

R35 10

C23 0µ1

2MHz TTL

ML12 DECADE DIVIDER

R41 10

C25 0µ1

TP9

10kHz TTL

DIVIDE-BY-100 CHAIN

TYPICAL AC VOLTAGE MEASURED WITH A HIGH IMPEDANCE VOLTMETER OR OSCILLOSCOPE

TYPICAL DC VOLTAGE MEASURED WITH A 20KΩ/V METER OR EQUIVALENT

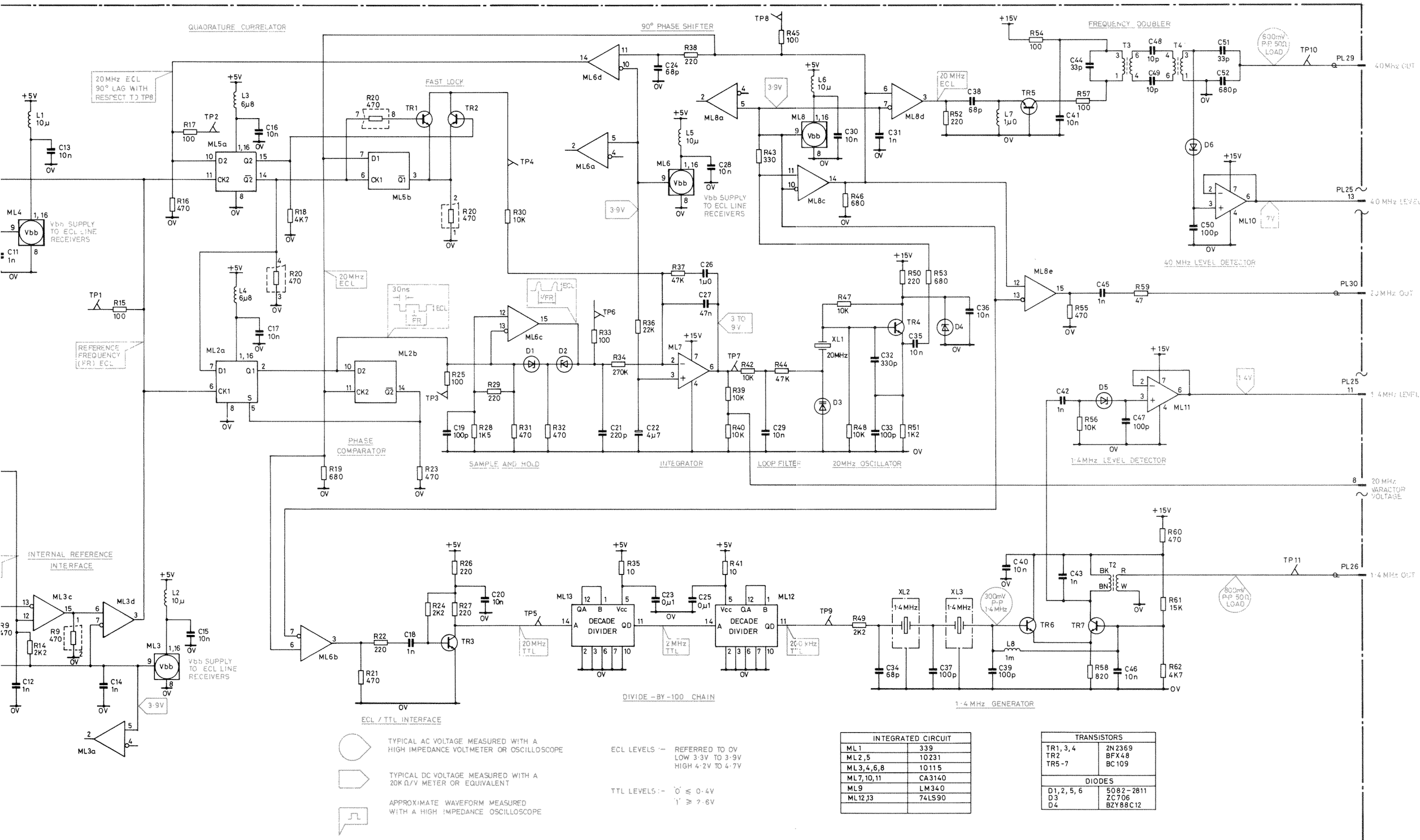
APPROXIMATE WAVEFORM MEASURED WITH A HIGH IMPEDANCE OSCILLOSCOPE

ECL LEVELS :- REFERRED TO OV
LOW 3·3V TO 3·9V
HIGH 4·2V TO 4·7V

TTL LEVELS :- '0' ≤ 0·4V
'1' ≥ 2·6V

RACAL

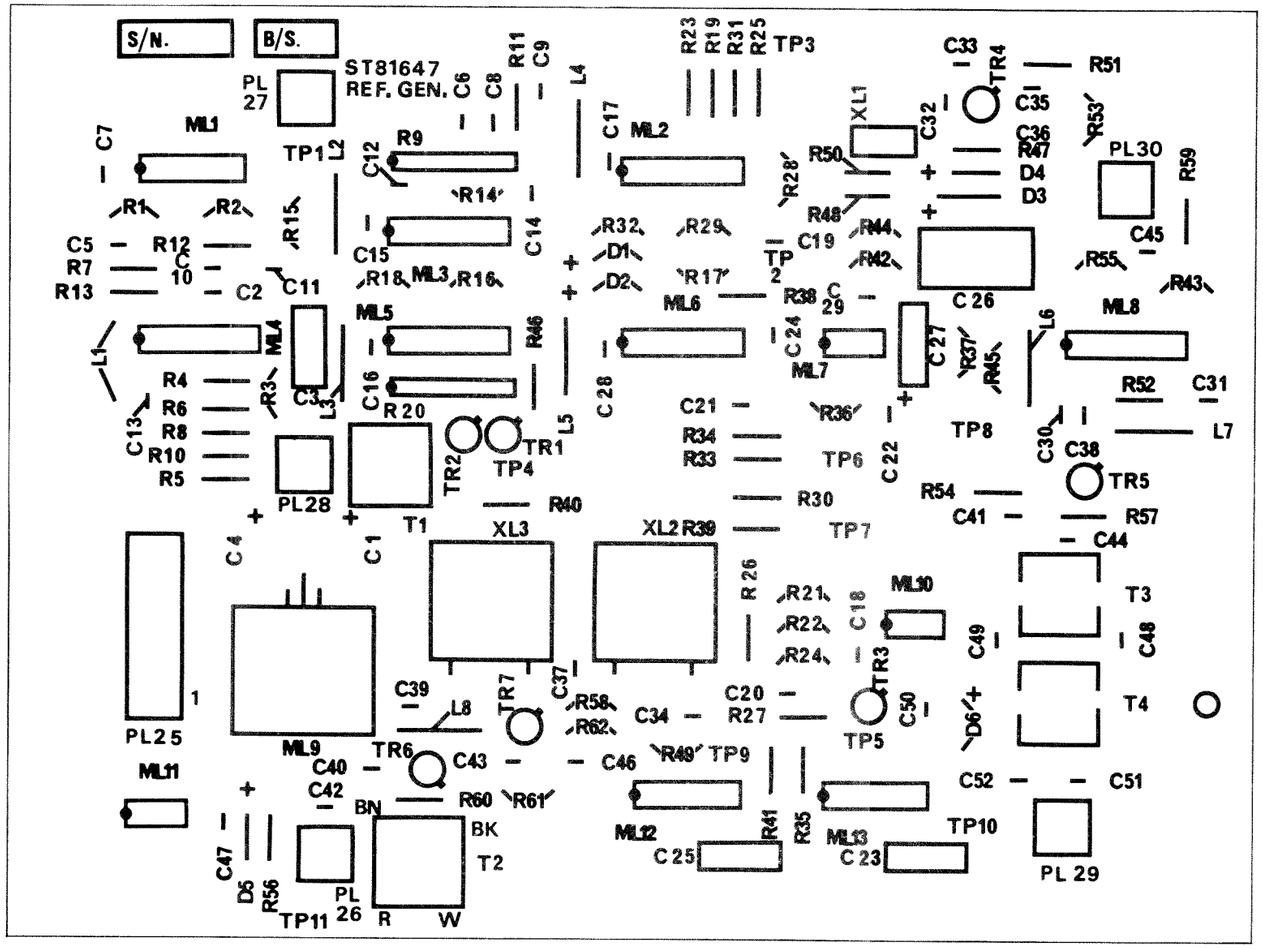
TH 3071	DC 81647	7.1
2		1/2



INTEGRATED CIRCUIT	
ML1	339
ML2,5	10231
ML3,4,6,8	10115
ML7,10,11	CA3140
ML9	LM340
ML12,13	74LS90

TRANSISTORS	
TR1,3,4 TR2 TR5-7	2N2369 BFX48 BC109
DIODES	
D1,2,5,6 D3 D4	5082-2811 ZC706 BZY88C12

Circuit : Reference Generator Board **Fig. 7.1**



RACAL

TH3071	DA8164674
1	

Layout : Reference Generator Board

Fig. 7-2

CHAPTER 8

SYNTHESIZER BOARD

CONTENTS

Tables

Illustrations

Text

At end of chapter

CHAPTER 8

SYNTHESIZER BOARD

INTRODUCTION

1. A single-loop synthesizer is used to produce the 42.4 MHz to 71.4 MHz local oscillator signal, which is applied to the mixer board. It makes use of an LSI device (ML12) which contains the synthesizer control circuitry. A simplified block diagram of this device is given in fig. 8(a).

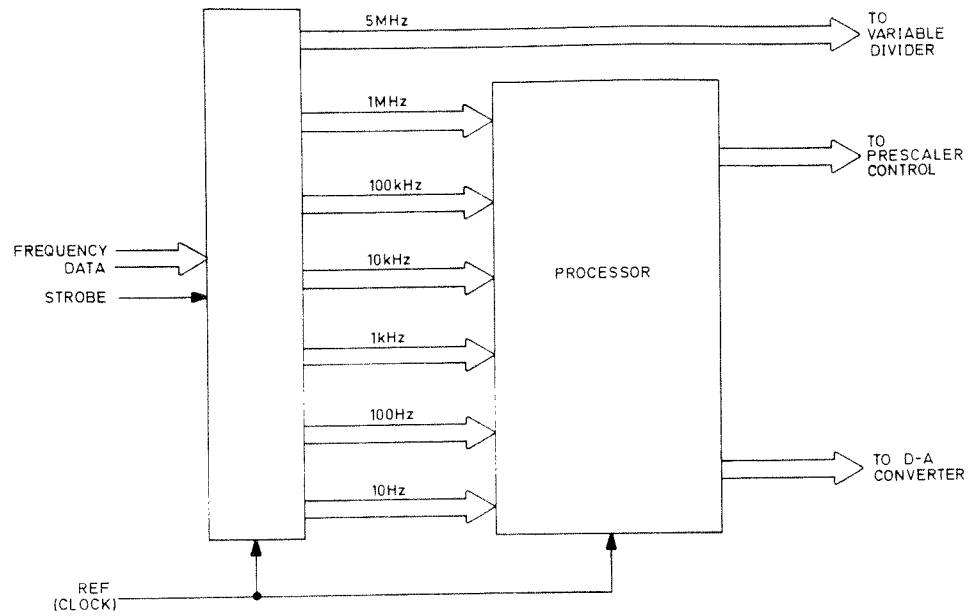


Fig. 8 (a) Block Diagram : Synthesizer Control Device ML12

FUNCTIONAL DESCRIPTION

2. In the block diagram of the synthesizer board given in fig. 8(b), the main signal flow is denoted by the heavy lines. An output signal from the 42.4 MHz to 71.4 MHz VCO (TR8) is applied to a phase comparator via a buffer amplifier TR1, TR2, TR3, a shaper stage ML5, and a programmed divider comprising a divide-by-5/divide-by-6 prescaler ML16 and a variable divider ML11 (both controlled by ML12) together with output buffer and reclocking stages ML10a, ML10b. A 1 MHz reference signal from the control stage ML12 is first re-synchronised to a 5 MHz signal derived from the 20 MHz reference signal, and is then applied as the second input to the phase comparator. The main output signal from the phase comparator is then applied to a pulse-width integrator (ML2a) to produce the varactor control voltage which is applied to the VCO via a summing node, a further integrator (ML3), and the loop amplifier ML2b.

3. Thus the phase comparator output signal drives the VCO until its frequency, when divided by the programmed divider, is equal to the 1 MHz reference frequency, and phase-lock is then achieved.

4. The division ratio to voltage conversion stage is fed from the $\overline{Q}$ output of the re-clocking stage ML10b, and produces an output voltage which is proportional to the programmed divider division ratio. This circuit is included to increase the effective phase comparator gain with an increasing division ratio and so maintain a constant loop bandwidth.

5. The fast lock circuit provides additional control only when the loop is out of lock. The output is summed with that from the pulse-width integrator and also that from a digital-to-analogue converter with differentiating capacitor C52. This latter stage is included to control the phase of the loop current and further reduce spurious levels.

6. The output signal from integrator stage ML3 is applied via loop amplifier ML2b to the varactor diodes of the VCO, and is also applied to a fast lock detector. This stage is used to detect a change in the drive unit frequency setting and then rapidly drives the VCO, either up or down, as necessary, to bring about a rapid return to the locked condition.

CIRCUIT DESCRIPTION (figs. 8.1 and 8.2)

Reference Input Shaper

7. The 20 MHz reference signal at PL32 is coupled by C14 to a wideband amplifier/limiter stage which uses all four sections of a quad line receiver device ML21. This is an ECL (emitter coupled logic) device and contains a Vbb supply generator which is used to set the input and output threshold levels (table 1).

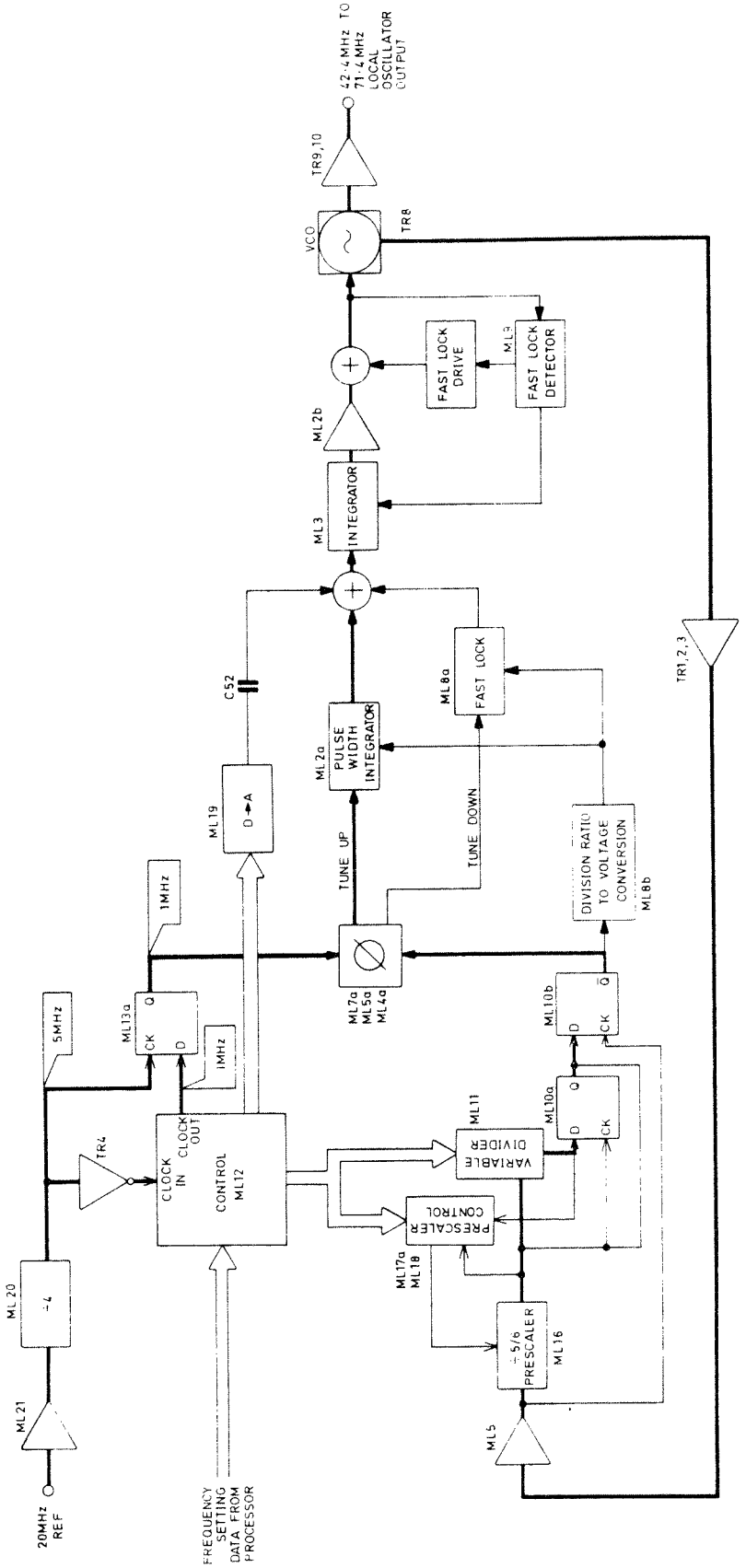


Fig. 8(b) Block Diagram : Synthesizer Board

Table 1 : Quad Line Receiver Truth Table

NON-INVERTING INPUT	INVERTING INPUT	OUTPUT
L	H	L
H	L	H
L	Vbb	L
H	Vbb	H
Vbb	H	L
Vbb	L	H

Divide-by-four Stage

8. The 20 MHz output signal from ML21d is applied to a divide-by-four stage consisting of an ECL high-speed dual D-type flip-flop ML20a, ML20b. The 5 MHz signal at the Q output of ML20b is converted to 9V C-MOS levels by TR4 before application to the digiphase synthesizer control stage ML12, whilst a 5 MHz output signal at ECL levels (from the $\overline{Q}$ output of ML20b) is applied to the 1 MHz reclocking stage ML13a.

9.1V C-MOS Supply

9. This is derived from the +15V supply (+12V regulator ML23, R10 and zener diode D1) and is routed to the supply pins of ML12 (Vdd), ML1 (GND) and ML19 (V+).

Programmed Divider

10. A 42.4 MHz to 71.4 MHz output signal from the VCO (para. 24) is applied via buffer amplifier stage TR1, TR2, TR3, and ECL shaper stage ML15, to the programmed divider comprising divide-by-5/divide-by-6 prescaler ML16, prescaler control stage ML18, ML17a, and main variable divider ML11, ML10a.

11. The prescaler stage ML16 is an ECL high speed device with a division ratio of 5 or 6 dependent on the level applied to the M1 and M2 mode control inputs (table 2). In addition to the ECL Q output (pin 8), which is used for VCO reclocking, an internal ECL-to-TTL converter provides a TTL Q output (pin 11), which is applied to the clock inputs of ML18, ML11 and ML10a. The prescaler control stage ML18 is a TTL presettable binary down counter (up/down input connected to 0V), where the mode of operation is determined by the state of the $\overline{\text{LOAD}}$, ENABLE $\overline{P}$ and ENABLE $\overline{T}$ control inputs. Both enable inputs must be at logic '0' for counting to take place, whilst a logic '0' pulse at the $\overline{\text{LOAD}}$ input temporarily disables the counter and causes the Q outputs to agree with the data inputs after the next clock pulse.

Table 2 : Prescaler Mode Control

INPUTS				OUTPUT RESPONSE
MS	$\overline{CE}$	M1	M2	
H	X	X	X	SET HIGH
L	H	X	X	HOLD
L	L	L	L	÷ 6
L	L	X	H	÷ 5
L	L	H	X	÷ 5

12. ML18 thus counts down from the preset number at the A, B, C and D input pins, and whilst this counting-down is in progress, because at least one of the QB, QC or QD outputs will be at logic '1', the output from NOR gate ML17a is maintained at a '0', ML18 is enabled, and ML16 divides by 6. When ML18 counts down to numeral 1 i.e. QB, QC and QD outputs all at '0', the output from ML17a changes to a '1', ML18 is disabled, and ML16 divides by 5. This condition is maintained until the application of the next preset-enable (LOAD) pulse from ML11, at which time the cycle is repeated.

13. The main programmed divider stage ML11 is also a TTL presettable binary down counter (up/down input connected to OV), which is permanently enabled by connecting both enable inputs to OV. It counts down from the preset number at the A, B, C and D input pins, and produces a negative-going pulse at the ripple-carry output (RCO) pin each time a count of zero is reached (fig. 8(c)). This output is applied via buffer stage ML10a to the VCO reclocking stage ML10b, and also to the $\overline{LOAD}$ input pins of ML18 and ML11 to prset-enable both counters.

D-A Converter

14. ML19 is an 8-bit high-speed multiplying digital-to-analogue converter where the output current is a product of the digital number and the input reference current. The full-scale output current is a linear function of the reference current, and is given by the expression:

$$Ifs = 255/256 \times Iref$$

where Iref is the input current at pin 14 (Vref+). The Vref+ and Vref- inputs are taken to the non-inverting and inverting inputs respectively of an internal reference amplifier. Since the Vref- input is taken to OV, the internal feedback maintains a low-impedance, virtual-earth at the Vref+ input pin, and establishes a OV reference at the junction of R68 and D13 (fig. 8.2). The protection diode D13 prevents the potential at pin 14 of ML19 rising above approximately 0.7V.

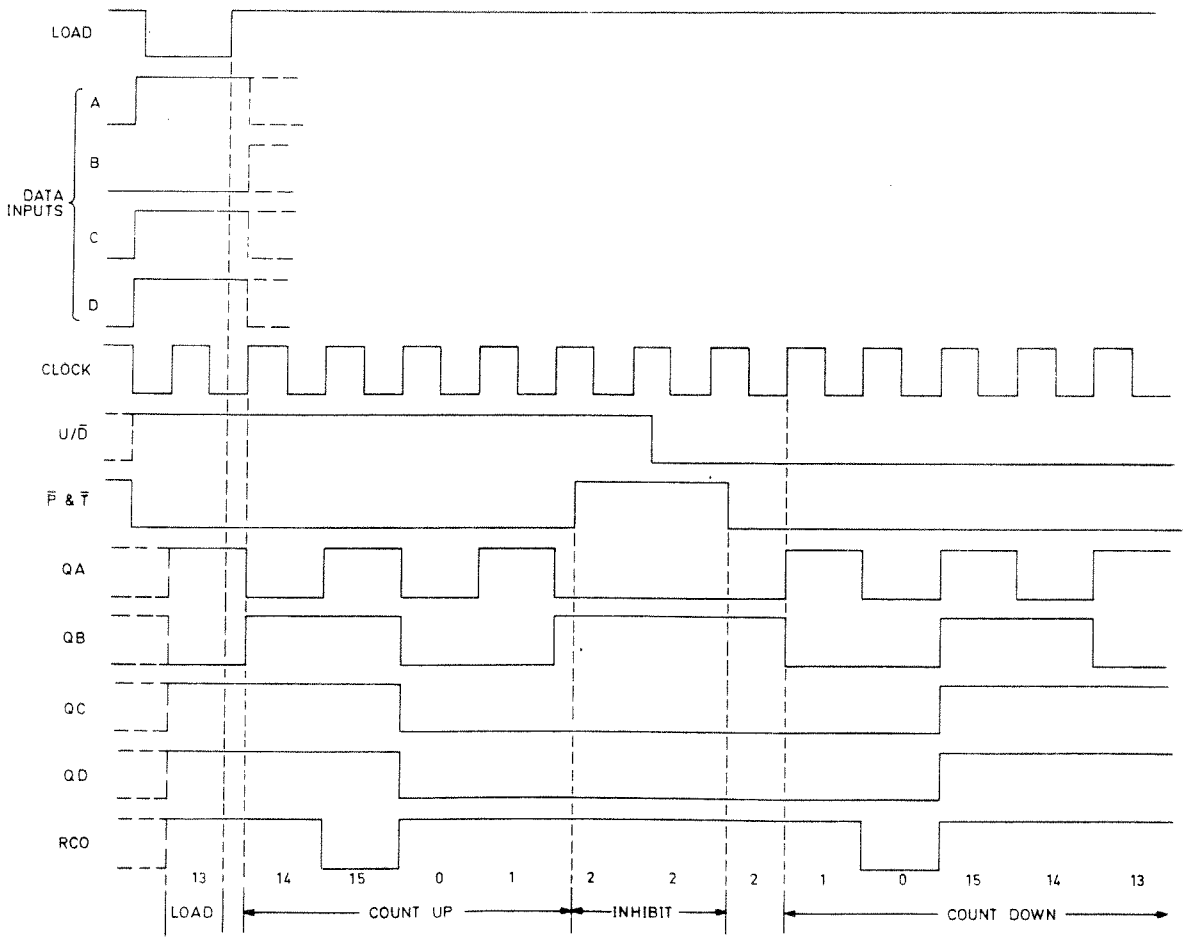


Fig. 8 (c) Timing Diagram : Presettable Binary Counter (74LS169)

Phase Comparator

15. The phase comparator uses two high-speed ECL D-type flip-flops ML5a, ML7a, together with NOR gate ML4a. The D inputs of the two flip-flops are taken to OV, the 1 MHz reference signal is used to clock ML5a, whilst ML7a is clocked by the output signal from the programmed divider. Thus when the positive-going edge of the 1 MHz signal at TP10 clocks ML5a, the '0' at the D input results in a '0' at the Q output, and this is applied to one input of ML4a. Similarly, when the positive-going edge of the programmed divider signal at TP9 clocks ML7a, the '0' at the D input results in a '0' at the Q output, and this is applied to the remaining input of ML4a. When both inputs of ML4a are at '0', a '1' is produced at the output, and this is used to set both ML5a and ML7b.

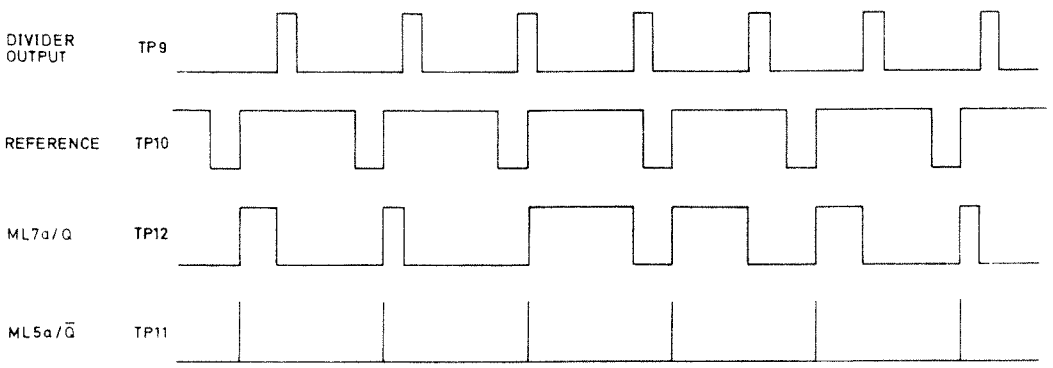


Fig. 8 (d) Timing Diagram : Divider Frequency High

16. The timing diagram given in fig. 8(d) shows the situation where the VCO frequency, and hence the divider output frequency, is too high. The resulting waveform at the Q output of ML7a (TP12) is applied to the fast-lock circuit ML8a, which causes a reduction in the VCO varactor voltage (and hence a reduction in the VCO frequency), as follows.

17. Under phase-locked conditions, the 4 nanosecond negative-going pulses at the Q output of ML7a (fig. 8(f)) are too fast to overcome the time constant presented by D9, R60, C48, and a voltage of approximately +3.8 V is established at the junction of D9 with D11. Current flow through D11 is thus prevented, whilst D12 is forward biased to allow ML8a to draw current from the summing node, the level of which is proportional to the output level from the division ratio to voltage converter stage ML8b (para. 21).

18. When the VCO frequency is too high, as depicted in fig. 8(d), the relatively wider negative-going pulses at the Q output of ML7a cause a reduction in the voltage level at the junction of D9 with D11, and ML8a draws current from the summing node via D11 and R60 to lower the VCO varactor voltage. At the same time, the very narrow positive-going pulses at the $\overline{Q}$ output of ML5a cause D8 to become forward biased, and any current produced by R59 is diverted from the summing node.

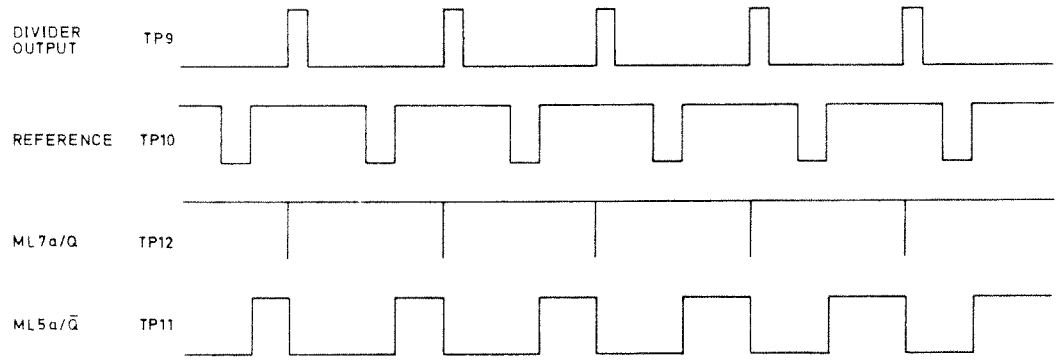


Fig. 8(e) Timing Diagram : Divider Frequency Low

19. The situation where the divider frequency is low is depicted in fig. 8(e). This time the wider positive-going pulses at the $\overline{Q}$ output of ML5a allow the current produced by R59 to flow into the summing node to raise the varactor voltage,and hence the VCO frequency. At the same time, the very narrow negative-going pulses at the Q output of ML7a prevent current drain from the summing node via D11 and R60.

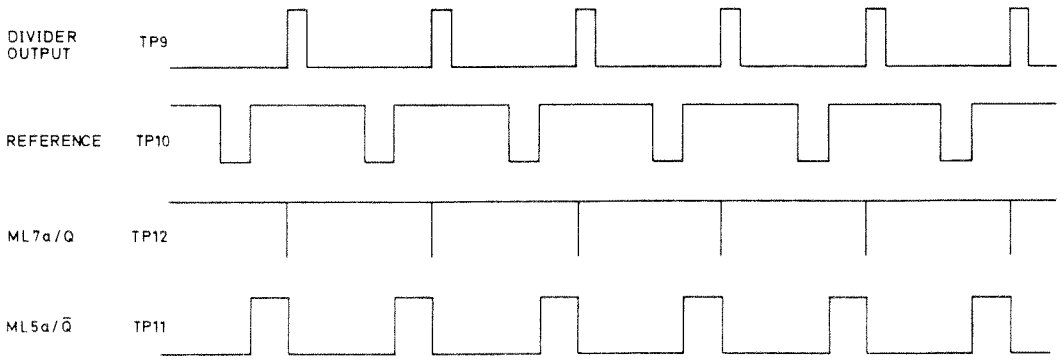


Fig. 8 (f) Timing Diagram : Divider & Reference In Phase

20. Fig. 8(f) depicts the in-lock condition, where the two signals are equal in frequency, and where the phasing is such that the duration of the pulses at TP11 is approximately 40 times the duration of the pulses at TP12 (160 nanoseconds and 4 nanoseconds respectively). The effect of this is such that under phase-locked conditions the current fed into the summing node from R59 is equal to that drawn from the node by ML8a, no current flows through R65, and a voltage is produced at the output of integrator stage ML3 (TP15) which is inversely proportional to the VCO frequency. This voltage is filtered, level-shifted, inverted and amplified by ML2b, and is then applied to the VCO varactor diodes via the loop filter (R83, R87, R88, R89, C63, C64), R92 and L10.

Division Ratio to Voltage Converter

21. This comprises ML8b and shottky diodes D6 and D7. The feedback loops around operational amplifier ML8b (a.c. feedback via C50, d.c. feedback via R62, R50 and D7) continually strive to maintain the inverting input at the 3.9 V reference level applied to the non-inverting input. Since the positive-going pulses at the $\overline{Q}$ output of ML10b are applied to D6, the higher the division ratio, the shorter the duration of the positive-going pulses, the lower the voltage at the inverting input of ML8b and consequently the higher the voltage at the output of ML8b.

Fast Lock Detector

22. This circuit, comprising ML9a, ML9b and ML9c, comes into operation following an abrupt change in the drive unit frequency setting. At all other times, the voltages from potential divider R84, R85, R86 ensure that a '1' is present at the outputs of both ML9a and ML9b (pull-up voltage from R93). This results in a voltage of approximately +20 V at the junction of R99 with D20, and the quad transmission gate ML1 is held disabled (ML1 is designed to be operated from plus and minus 15 V supplies. In this application however, the minus supply conection is taken to 0 V, the 0 V connection is taken to +9.1 V, and the positive connection is taken to +20 V. This means that, as far as ML1 is concerned, a level of +20 V at a control input is regarded as a logic '1', to inhibit switch operation, whilst a level of approximately +9 V is regarded as a logic '0', to enable switch operation).

23. When a change of drive unit frequency occurs, the voltage at the output of loop amplifier ML2b is abruptly taken high for an increase in frequency, or low for a decrease in frequency. This abrupt change is sensed by the limit comparator formed by ML9a and ML9b such that if the level applied to ML9a pin 10/ML9b pin 8 exceeds +18 V or falls below +1.6 V, then the output from either ML9a or ML9b is pulled down to 0 V. This results in a '0' at the output of ML9c (TP 20) and this is translated to a level of approximately +9 V to enable quad transmission gate ML1. The three sections of ML1 (a, b and c) close to increase the bandwidth of the loop filter and also to being the fast lock driver stage ML6, TR6, TR7 into operation, to bring about a rapid return to the phase-locked condition.

42.4 MHz to 71.4 MHz VCO

24. The VCO comprises a low-noise, N-chanel FET TR8, tapped inductor L11, and a pair of varactor diodes, D17 and D18. The output signal applied to the programmed divider is taken from the drain of TR8, whilst that fed to the mixer board is taken from a low-impedance tap on L11 and is coupled by C71 to the cascode output amplifier stage TR9, TR10. D21 and voltage-follower stage ML14 provide a d.c. output signal proportional in amplitude to that of the local oscillator output signal, and this is routed to the processor board for test purposes.

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
		SYNTHESIZER BOARD (ST 81645)			
Resistors					
R1	10	Metal Oxide		2	920736
R2	100	Metal Oxide		2	910388
R3	1 k	Metal Oxide		2	913489
R4	100	Metal Oxide		2	910388
R5	100	Metal Oxide		2	910388
R6	470	Metal Oxide		2	920758
R7	100	Variable, preset			923661
R8	39	Metal Oxide		2	917062
R9	2k2	Metal Oxide		2	916546
R10	100	Metal Oxide		2	910388
R11	100	Metal Oxide		2	910388
R12	56	Metal Oxide		2	917055
R13	10	Metal Oxide		2	920736
R14	10	Metal Oxide		2	920736
R15	1 k	Metal Oxide		2	913489
R16	470	Metal Oxide		2	920758
R17	470	Metal Oxide		2	920758
R18	100	Metal Oxide		2	910388
R19	470	Metal Oxide		2	920758
R20	470	Metal Oxide		2	920758
R21	470	Metal Oxide		2	920758
R22	470	Metal Oxide		2	920758
R23	470	Metal Oxide		2	920758
R24	470	Metal Oxide		2	920758
R25	470	Metal Oxide		2	920758
R26	470	Metal Oxide		2	920758
R27	470	Metal Oxide		2	920758
R28	100	Metal Oxide		2	910388
R29	470	Metal Oxide		2	920758
R30	470	Metal Oxide		2	920758
R31	10 k	Metal Oxide		2	914042
R32	220	Metal Oxide		2	910390
R33	1 k	Metal Oxide		2	913489
R34	10 k	Metal Oxide		2	914042
R35	2k2	Metal Oxide		2	916546
R36	820	Metal Oxide		2	917065
R37	820	Metal Oxide		2	917065
R38	220	Metal Oxide		2	910390
R39	220	Metal Oxide		2	910390
R40	470	Metal Oxide		2	920758

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
R41	3k3	Metal Oxide		2	910111
R42	150	Metal Oxide		2	910389
R43	100	Variable, preset			923661
R44	470	Metal Oxide		2	920758
R45	470	Metal Oxide		2	920758
R46	100	Metal Oxide		2	910388
R47	100	Metal Oxide		2	910388
R48	470	Metal Oxide		2	920758
R49	270	Metal Oxide		2	910391
R50	2k2	Metal Oxide		2	916546
R51	470	Metal Oxide		2	920758
R52	470	Metal Oxide		2	920758
R53	470	Metal Oxide		2	920758
R54	22 k	Metal Oxide		2	913493
R55	10 k	Metal Oxide		2	914042
R56	68 k	Metal Oxide		2	916478
R57	1 k	Metal Oxide		2	913489
R58	1 k	Metal Oxide		2	913489
R59	10 k	Metal Oxide		2	914042
R60	3k3	Metal Oxide		2	910111
R61	22 k	Metal Oxide		2	913493
R62	100	Metal Oxide		2	910388
R63	22 k	Metal Oxide		2	913493
R64	1 k	Metal Oxide		2	913489
R65	22	Metal Oxide		2	920743
R66	15 k	Metal Oxide		2	920645
R67	390	Metal Oxide		2	916331
R68	1k2	Metal Oxide		2	911179
R69	1 k	Metal Oxide		2	913489
R70	15 k	Metal Oxide		2	920645
R71	100	Metal Oxide		2	910388
R72	47 k	Metal Oxide		2	913496
R73	10 k	Metal Oxide		2	914042
R74	12 k	Metal Oxide		2	921771
R75	10 k	Metal Oxide		2	914042
R76	10 k	Metal Oxide		2	914042
R77	18 k	Metal Oxide		2	900994
R78	15 k	Metal Oxide		2	920645
R79	15 k	Metal Oxide		2	920645
R80	10 k	Metal Oxide		2	914042

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
R81	47 k	Metal Oxide		2	913496
R82	120	Metal Oxide		2	920751
R83	220 k	Metal Oxide		2	921771
R84	1 k	Metal Oxide		2	913489
R85	6k8	Metal Oxide		2	910112
R86	680	Metal Oxide		2	910113
R87	10	Metal Oxide		2	920736
R88	680	Metal Oxide		2	910113
R89	22	Metal Oxide		2	920743
R90	2k2	Metal Oxide		2	916546
R91	2k2	Metal Oxide		2	916546
R92	100	Metal Oxide		2	910388
R93	39 k	Metal Oxide		2	900993
R94	220 k	Metal Oxide		2	921771
R95	47	Metal Oxide		2	917036
R96	68	Metal Oxide		2	916476
R97	68	Metal Oxide		2	916476
R98	15 k	Metal Oxide		2	920645
R99	10 k	Metal Oxide		2	914042
R100	390	Metal Oxide		2	916331
R101	1 k	Metal Oxide		2	913489
R102	680	Metal Oxide		2	910113
R103	22	Metal Oxide		2	920743
R104	10	Metal Oxide		2	920736
R105	56	Metal Oxide		2	917055
R106	10 k	Metal Oxide		2	914042
R107	10 k	Metal Oxide		2	914042
R108	3k3	Metal Oxide		2	910111
R109	1 k	Metal Oxide		2	913489
Capacitors			V		
C1	4µ7	Tantalum Bead	35	20	914026
C2	4µ7	Tantalum Bead	35	20	914026
C3	1µ0	Tantalum Bead	35	20	939585
C4	1µ0	Tantalum Bead	35	20	939585
C5	1 n	Ceramic Disc	500	20	915243

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
C6	4µ7	Tantalum Bead	35	20	914026
C7	4µ7	Tantalum Bead	35	20	914026
C8	10 n	Ceramic Disc	250	+40 -20	900067
C9	1 n	Ceramic Disc	500	20	915243
C10	10 n	Ceramic Disc	250	+40 -20	900067
C11	0µ1	Polycarbonate	100	10	931130
C12	10 p	Ceramic Disc	500	5	921270
C13	1µ0	Tantalum Bead	35	20	923565
C14	1 n	Ceramic Disc	500	20	915243
C15	1µ0	Tantalum Bead	35	20	939585
C16	1 n	Ceramic Disc	500	20	915243
C17	10 n	Ceramic Disc	250	+40 -20	900067
C18	4µ7	Tantalum Bead	35	20	914026
C19	10 n	Ceramic Disc	250	+40 -20	900067
C20	0µ1	Polycarbonate	100	10	931130
C21	1µ0	Tantalum Bead	35	20	939585
C22	1 n	Ceramic Disc	500	20	915243
C23	0µ1	Polycarbonate	100	10	931130
C24	10 n	Ceramic Disc	250	+40 -20	900067
C25	1 n	Ceramic Disc	500	20	915243
C26	10 n	Ceramic Disc	250	+40 -20	900067
C27	10 n	Ceramic Disc	250	+40 -20	900067
C28	6µ8	Tantalum Tubular	40	10	931178
C29	1 n	Ceramic Disc	500	20	915243
C30	10 n	Ceramic Disc	250	+40 -20	900067
C31	10 n	Ceramic Disc	250	+40 -20	900067
C32	10 n	Ceramic Disc	250	+40 -20	900067
C33	6µ8	Tantalum Tubular	40	10	931178
C34	10 n	Ceramic Disc	250	+40 -20	900067
C35	1 n	Ceramic Disc	500	20	915243
C36	10 n	Ceramic Disc	250	+40 -20	900067
C37	0µ1	Polycarbonate	100	10	931130
C38	10 n	Ceramic Disc	250	+40 -20	900067
C39	10 n	Ceramic Disc	250	+40 -20	900067
C40	6µ8	Tantalum Tubular	40	10	931178
C41	10 n	Ceramic Disc	250	+40 -20	900067
C42	10 n	Ceramic Disc	250	+40 -20	900067
C43	6µ8	Tantalum Tubular	40	10	931178
C44	10 n	Ceramic Disc	250	+40 -20	900067
C45	6µ8	Tantalum Tubular	40	10	931178

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
C46	1 n	Ceramic Disc	500	20	915243
C47	0µ1	Polycarbonate	100	10	931130
C48	100 p	Ceramic Disc	500	10	917417
C49	1µ0	Tantalum Bead	35	20	939585
C50	1µ0	Tantalum Bead	35	20	939585
C51	100 p	Ceramic Disc	500	10	917417
C52	22 p	Ceramic Disc	500	5	940026
C53	10 n	Ceramic Disc	250	+40 -20	900067
C54	100 p	Ceramic Disc	500	10	917417
C55	10 n	Ceramic Disc	250	+40 -20	900067
C56	4µ7	Tantalum Bead	35	20	914026
C57	47n	Polycarbonate	250	10	935141
C58	1n5	Tantalum Bead	35	20	914026
C60	1 n	Ceramic Disc	250	+40 -20	900067
C61	1 n	Ceramic Disc	500	20	915243
C62	1 n	Ceramic Disc	500	20	915243
C63	1µ0	Tantalum Bead	35	20	923565
C64	33 n	Polycarbonate	250	10	939695
C65	0µ1	Polycarbonate	100	10	931130
C66	4µ7	Tantalum Bead	35	20	914026
C67	10 n	Ceramic Disc	250	+40 -20	900067
C68	1 n	Ceramic Disc	500	20	915243
C69	1 n	Ceramic Disc	500	20	915243
C70	6µ8	Tantalum Tubular	40	10	931178
C71	1 n	Ceramic Disc	500	20	915243
C72	4µ7	Tantalum Bead	35	20	914026
C73	10 n	Ceramic Disc	250	+40 -20	900067
C74	1 n	Ceramic Disc	500	20	915243
C75	10 p	Ceramic Disc	500	5	921270
C76	1 n	Ceramic Disc	500	20	915243
C77	0µ1	Polycarbonate	100	10	931130
C78	4µ7	Tantalum Bead	35	20	914026
C79	1 n	Ceramic Disc	500	20	915243

Inductors

L1	15 µH	Choke		10	938955
L2	0µ47H	Choke		10	939693
L3	15 µH	Choke		10	938955
L4	1 µH	Choke		10	938966
L5	47 µH	Choke		10	939160

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
L6	1 µH	Choke		10	938966
L7	0µ47H	Choke		10	939693
L8	1 µH	Choke		10	938966
L9	1µ5H	Choke		10	938967
L10	6µ8H	Choke		10	939694
L11		Coil Assembly			AT82406

Transformers

T1		Transformer Assembly			AT82407

Connectors

PL31		Plug, 20-way			939969
PL32		Plug, Coaxial, 50 ohms			935268
PL33		Plug, Coaxial, 50 ohms			935268

Diodes

D1		Zener, 9.1 V, 400 mW, BZX79C9V1			921751
D2		Silicon 1N4001			923563
D3		Schottky, HP5082-2811			919460
D4		Silicon 1N4149			923222
D5		Silicon 1N4149			923222
D6		Schottky, HP5082-2811			919460
D7		Schottky, HP5082-2811			919460
D8		Schottky, HP5082-2811			919460
D9		Silicon 1N4149			923222
D10		Schottky, HP5082-2811			919460
D11		Silicon 1N4149			923222
D12		Silicon 1N4149			923222
D13		Silicon 1N4149			923222
D14		Silicon 1N4149			923222
D15		Silicon 1N4149			923222

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
D16		Silicon 1N4149			923222
D17		Varactor, DKV6522B			925082
D18		Varactor, DKV6522B			925082
D19		Silicon 1N4149			923222
D20		Silicon 1N4149			923222
D21		Schottky, HP5082-2811			919460

Transistors

TR1		NPN Silicon 2N2369			906842
TR2		NPN Silicon 2N2369			906842
TR3		NPN Silicon 2N2369			906842
TR4		NPN Silicon 2N2369			906842
TR5		NPN Silicon BC109			923234
TR6		NPN Silicon BC109			923234
TR7		PNP Silicon ZTX550L			937503
TR8		N-Channel FET 2N3823			938592
TR9		NPN Silicon 2N3866			917219
TR10		NPN Silicon 2N3866			917219

Integrated Circuits

ML1		Quad transmission gate DG201			934880
ML2		Quad Operational amplifier 324			933619
ML3		Operational amplifier AD518J			935269
ML4		Quad 2-input NOR gate 10102P			938873
ML5		Dual D-type flip-flop 10231P			938877
ML6		Operational amplifier CA3140E			932204
ML7		Dual D-type flip-flop 10231P			938877
ML8		Quad operational amplifier 324			933619
ML9		Quad Comparator 339			925952
ML10		Dual D-type flip-flop 10231P			938877
ML11		Binary Counter 74LS169			939895
ML12		Digiphase Processor RMSL019/A			AD80763
ML14		Operational amplifier CA3140E			932204
ML15		Quad line receiver 10115P			938874

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
ML16		Prescaler F11C91DC			939928
ML17		Triple 3-input NOR gate 74LS27			931631
ML18		Binary Counter 74LS169			939895
ML19		D-A Converter DAC08			939896
ML20		Dual D-type flip-flop 10231P			938877
ML21		Quad line receiver 10115P			938874
ML22		+5 V Regulator LM340T5			939921
ML23		+12 V Regulator 7812CT			933987

Miscellaneous

		Test Point			936148
		Captive fastener			930396
		Heatsink (for ML22)			BD82536
		8-pin DIL IC socket			940901
		14-pin DIL IC socket			940902
		16-pin DIL IC socket			940903
		40-pin DIL IC socket			930613

SYNTHESIZER BOARD (ST 83715)

(Fitted to some units instead of ST 81645)

Synthesizer Board ST 83715 differs from ST 81645 as follows:

R32 is deleted
C80 1n Ceramic Disc 500 20 915243 is added
ML16 is Prescaler MC12012P 941051
Connections are as shown in Fig. 8.1 inset.

REFERENCE INPUT SHAPER

DIVIDE-BY-4 STAGE

ALTERNATIVE CIRCUIT FOR EQUIPMENT FITTED WITH SYNTHESIZER BOARD ST8371.5

VCO BUFFER AMPLIFIER

ECL SHAPER STAGE

PROGRAMMED DIVIDER

20 MHz REFERENCE I/P

PL32

PL31

+12V REGULATOR ML23

+5V REGULATOR ML22

R7 IS ADJUSTED FOR +5.2V ± 50mV AT TP1

ML21a ML21b ML21c ML21d ML21 ML20a ML20b

ML15a ML15b ML15c ML15d ML15

ML16 QTTL PRESCALER ÷5/÷6

ML18 PRESETTABLE BINARY COUNTER

ML17a

OSCILLATOR FREQUENCY ECL LEVELS

1MHz STEPS

DIGIPHAS SYNTHESIZ CONTROL

RACAL

TH 3071	DC 81645 SHT 1	8.1
2		1/2

TH 3071	DC 81645 SHT 1	8.1
2		2/2

REFERENCE INPUT SHAPER

DIVIDE-BY-4 STAGE

REFERENCE RECLOCKING

ML12 DIGIPHASE SYNTHESIZER CONTROL

ML19 D-A CONVERTER

TO ADJUST R43
1 SET FREQUENCY TO 15·6010 MHz
2 SELECT "TUNE"
3 CONNECT AN OSCILLOSCOPE, AC COUPLED, SENSITIVITY ≥ 5mV/DIVISION, 2ms SWEEP, BETWEEN TP16 AND GROUND (TP 17)
4 SHORT TP7 TO GROUND (TP 3)
5 TRIGGER FROM TP5
6 ADJUST R43 FOR MINIMUM TRACE AMPLITUDE.

ALTERNATIVE CIRCUIT FOR EQUIPMENT FITTED WITH SYNTHESIZER BOARD ST83715

ML23

ML22

AMPLIFIER

ECL SHAPER STAGE

PROGRAMMED DIVIDER

OSCILLATOR FREQUENCY ECL LEVELS

1MHz STEPS

5MHz STEPS

'0' TO PRESET COUNTERS

VCO RECLOCKING

PRESCALER ÷5/÷6

PRESETTABLE BINARY COUNTER

D-A OUTPUT

D-A REFERENCE INPUT.

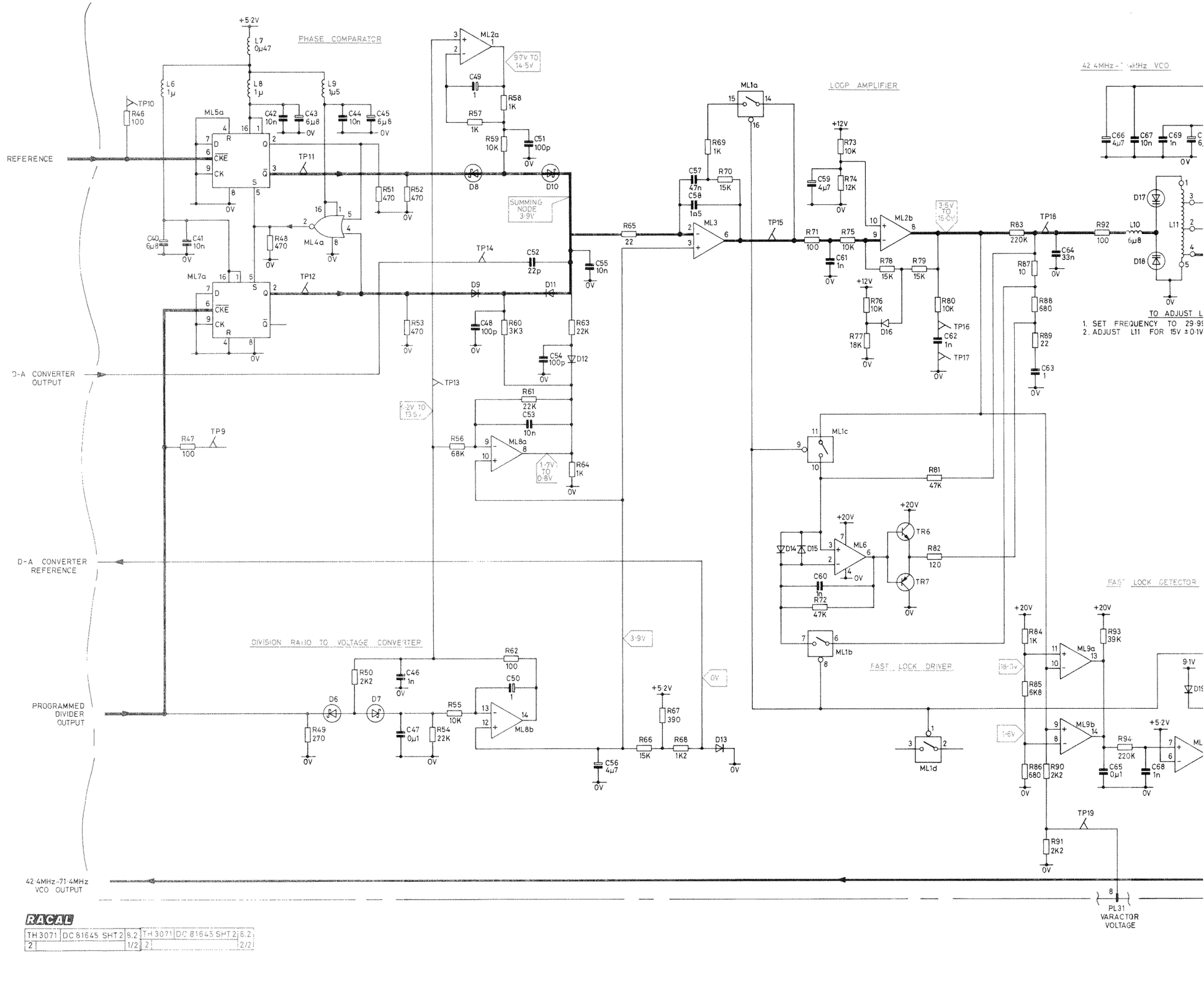
PHASE COMPARATOR REFERENCE

PHASE COMPARATOR V.C.O.

42·4MHz-71·4MHz V.C.O. OUTPUT

Circuit : Synthesizer Board (Sheet 1)

Fig. 8.1



TH3071	DC81645 SHT2	8.2	TH3071	DC81645 SHT2	8.2
2		1/2	2		2/2

PHASE COMPARATOR

LOOP AMPLIFIER

42·4MHz-71·4MHz VCO

OUTPUT AMPLIFIER

FAST LOCK DETECTOR

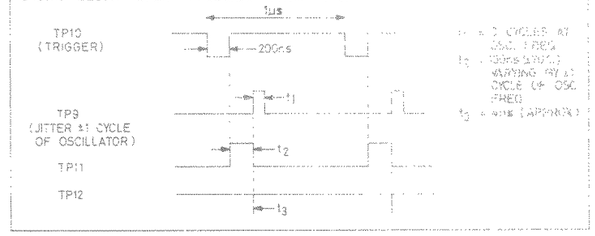
FAST LOCK DRIVER

DIVISION RATIO TO VOLTAGE CONVERTER

TO ADJUST L11

1. SET FREQUENCY TO 29·99999MHz.
2. ADJUST L11 FOR 15V ±0·1V AT TP16.

WHEN IN LOCK WAVEFORMS AT TP9,10,11,12 SHOULD BE AS SHOWN BELOW WHEN TRIGGERED FROM TP10.-



ECL LEVELS
'1' ≥ 4·3V
'0' ≤ 3·5V

TTL LEVELS
'1' ≥ 2·4V
'0' ≤ 0·8V

±20% DC VOLTAGE MEASURED WITH A 20KΩ/V METER ON EQUIVALENT

±3dB AC VOLTAGE MEASURED WITH A HIGH IMPEDANCE RF MILLIVOLTMETER OR SCOPE

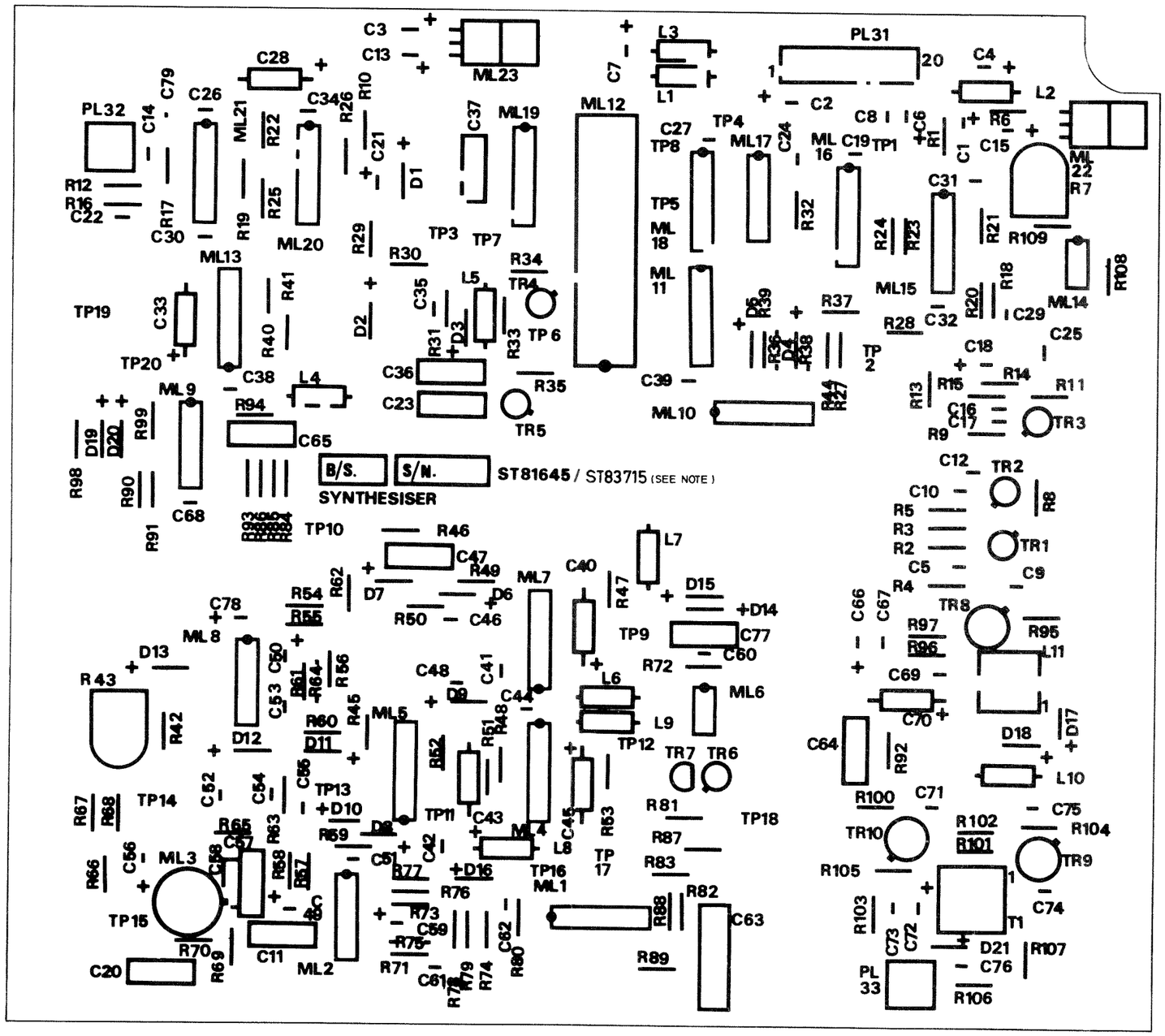
INTEGRATED CIRCUITS								
REF	TYPE	0V	5V(A)	5·2V	12V	20V	9·1V	-15V
ML1	DG201	4				13	5	
ML2,8.	324	11				4		
ML3	AD518	4			7			
ML4	10102	8		1,16 (L7,9)				
ML5	10231	8		1,16 (L7,8)				
ML6	3140	4				7		
ML7	10231	8		1,16 (L6,7)				
ML9	339	12				3		
ML10	10231	8		1,16.				
ML11,18.	74LS169	8	16					
ML12	RMSL019A	24		39			38	
ML13	10231	8	1,16.					
ML14	3140	4			7			
ML15	10115	8		1,16.				
* ML16	F11C91	12,13		4,5.				
ML17	74LS27	7		14				
ML19	DAC08	1					13	3
ML20	10231	8		1,16 (L4)				
ML21	10115	8	1,16					
ML22	LM340T5							
ML23	7812							

* ON BOARD ST83715 ML16 IS TYPE MC12012P

TRANSISTORS	
TR1,2,3,4.	2N2369
TR5,6	BC109
TR7	BFX 48
TR8	BFW 11
TR9,10.	2N3866
DIODES	
D1	BZY88C9V1
D2	IN4001
D3,6,7,8,10,21	HP5082-2811
D4,5,9,11,13,16,19,20.	IN4149
D17,18.	DKV6522B

Circuit: Synthesizer Board (Sheet 2)

Fig. 8.2



NOTE: ON ST83715 R32 IS REPLACED BY C80

RACAL

TH 3071	EA 81644/4	EA8371 4/4
2		1

Layout : Synthesizer Board **Fig. 8.3**

CHAPTER 9

MIXER BOARD

CONTENTS

Illustrations

CHAPTER 9

MIXER BOARD

INTRODUCTION

1. The mixer board accepts the 1.4 MHz output signal from the modulation board, mixes it with the 40 MHz signal from the reference generator board to produce an IF signal at 41.4 MHz, and then mixes this with the 42.4 MHz to 71.4 MHz local oscillator signal to produce a 1 MHz to 30 MHz output signal.

2. Four removeable links LK1 to LK4 are fitted at various points along the signal path to facilitate testing and alignment.

CIRCUIT DESCRIPTION (Fig. 9.1)

3. The 1.4 MHz signal from the modulation board, at coaxial connector PL17, is applied via impedance matching 6 dB pad R1, R3, R4 to the first mixer stage comprising T1, matched Schottky diodes D1A to D1D and T2. The 40 MHz reference signal at PL18 is amplified by TR1 and TR2 to provide the required drive as the mixer switching signal, and this is applied to the diode ring via T2. The mixer output signal is taken from T1 and is routed via link LK1, capacitor C4 and buffer amplifier stage TR3 to a band pass filter which selects the 41.4 MHz sum output frequency.

4. The gain of the first IF amplifier stage TR4, TR5 is preset by R26, and the output is transformer coupled to a 41.4 MHz crystal band pass roofing filter XL1, XL2 which has a nominal 3 dB bandwidth of 15 kHz. The filtered 41.4 MHz signal is then applied via a 2 dB pad R27, R29, R30 to the final mixer stage T4, TR8 to TR11 and T6, where it is mixed with 42.4 MHz to 71.4 MHz drive signal from differential amplifier stage TR6, TR7. The difference frequency output signal, in the range 1 MHz to 30 MHz, is applied via a low pass filter to the broadband output amplifier stage TR12, TR13. The output level detector formed by D3 and operational amplifier ML1 provides a d.c. output signal proportional to the RF level at TP11; this d.c. signal is routed to the processor board for test purposes.

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
		MIXER BOARD (ST 81651)			
Resistors			Watts		
R1	150	Metal Oxide	0.25	2	910389
R2	82	Metal Oxide	0.25	2	917057
R3	39	Metal Oxide	0.25	2	917062
R4	68	Metal Oxide	0.25	2	916476
R5	10	Metal Oxide	0.25	2	920736
R6	150	Metal Oxide	0.25	2	910389
R7	150	Metal Oxide	0.25	2	910389
R8	2k2	Metal Oxide	0.25	2	916546
R9	1k5	Metal Oxide	0.25	2	911166
R10	47	Metal Oxide	0.25	2	910763
R11	220	Metal Oxide	0.25	2	909549
R12	56	Metal Oxide	0.25	2	917055
R13	2k2	Metal Oxide	0.25	2	916456
R14	1k	Metal Oxide	0.25	2	913489
R15	47	Metal Oxide	0.25	2	910763
R16	22	Metal Oxide	0.25	2	920743
R17	270	Metal Oxide	0.25	2	910391
R18	10	Metal Oxide	0.25	2	920736
R19	10	Metal Oxide	0.25	2	920736
R20	47	Metal Oxide	0.25	2	910763
R21	100	Metal Oxide	0.25	2	920388
R22	1k	Metal Oxide	0.25	2	913489
R23	470	Metal Oxide	0.25	2	920758
R24	220	Metal Oxide	0.25	2	910390
R25	220	Metal Oxide	0.25	2	910390
R26	100	Variable, Preset	0.5	20	923661
R27	470	Metal Oxide	0.25	2	920758
R28	47	Metal Oxide	0.25	2	910763
R29	12	Metal Oxide	0.25	2	920738
R30	470	Metal Oxide	0.25	2	920758
R31	100	Metal Oxide	0.25	2	910763
R37	270k	Metal Oxide	0.25	2	923598
R38	220	Metal Oxide	0.25	2	910390
R39	10 k	Metal Oxide	0.25	2	914042
R40	1k	Metal Oxide	0.25	2	907731
R41	270	Metal Oxide	0.25	2	910391
R42	100	Metal Oxide	0.25	2	910388
R43	220	Metal Oxide	0.25	2	910390
R44	47k	Metal Oxide	0.25	2	913496
R45		Not Used			

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
R46	47	Metal Oxide	0.25	2	910763
R47	100k	Metal Oxide	0.25	2	915190
R48	100k	Metal Oxide	0.25	2	915190
Capacitors			**Volts**		
C1	10n	Ceramic Disc	250	+40 -20	900067
C2	0µ1	Polycarbonate	100	10	931130
C3	10n	Ceramic Disc	250	+40 -20	900067
C4	10n	Ceramic Disc	250	+40 -20	900067
C5	0µ1	Polycarbonate	100	10	931130
C6	10n	Ceramic Disc	250	+40 -20	900067
C7	12 p	Ceramic Disc	500	5	920511
C8	27 p	Ceramic Disc	500	5	939884
C9	2p2	Ceramic Disc	500	0.5 p	917734
C10	12 p	Ceramic Disc	500	5	920511
C11	56 p	Ceramic Disc	500	5	939885
C12	2p2	Ceramic Disc	500	0.5 p	917734
C13	27 p	Ceramic Disc	500	5	939884
C14	12 p	Ceramic Disc	500	5	920511
C15	10n	Ceramic Disc	250	+40 -20	900067
C16	0µ1	Polycarbonate	100	10	931130
C17	10n	Ceramic Disc	250	+40 -20	900067
C18	22 p	Ceramic Disc	500	5	939886
C19	5p6	Ceramic Disc	500	0.5 p	920876
C20	4-40 p	Trimmer			926275
C21	22 p	Ceramic Disc	500	5	939886
C22	10 p	Ceramic Disc	500	5	921270
C23	22 p	Ceramic Disc	500	5	939886
C24	10n	Ceramic Disc	250	+40 -20	900067
C25	0µ1	Polycarbonate	100	10	931130
C26	0µ1	Polycarbonate	100	10	931130
C27	0µ1	Polycarbonate	100	10	931130
C28	0µ1	Polycarbonate	100	10	931130
C29	0µ1	Polycarbonate	100	10	931130
C30	100 p	Ceramic Disc	500	10	917417
C31	120 p	Silver Mica	100	1	939888
C32	6p8	Ceramic Disc	500	0.5 p	919457
C33	1 n	Ceramic Disc	500	20	915243
C34	180 p	Silver Mica	100	2	900067
C35	0µ1	Polycarbonate	100	10	931130

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
C36	39 p	Silver Mica	400	1 p	906820
C37	150 p	Silver Mica	100	2	931614
C37	47 p	Silver Mica	400	1p	905203
C39	150 p	Silver Mica	100	2	931614
C40		Not Used			
C41	1µ0	Tantalum Bead	35	20	923571
C42	22 p	Silver Mica	400	1 p	930803
C43	0µ1	Polycarbonate	100	10	931130
C44	0µ1	Polycarbonate	100	10	931130
C45	100 p	Silver Mica	400	2	931736
C46	1 n	Ceramic Disc	500	20	915243

Inductors

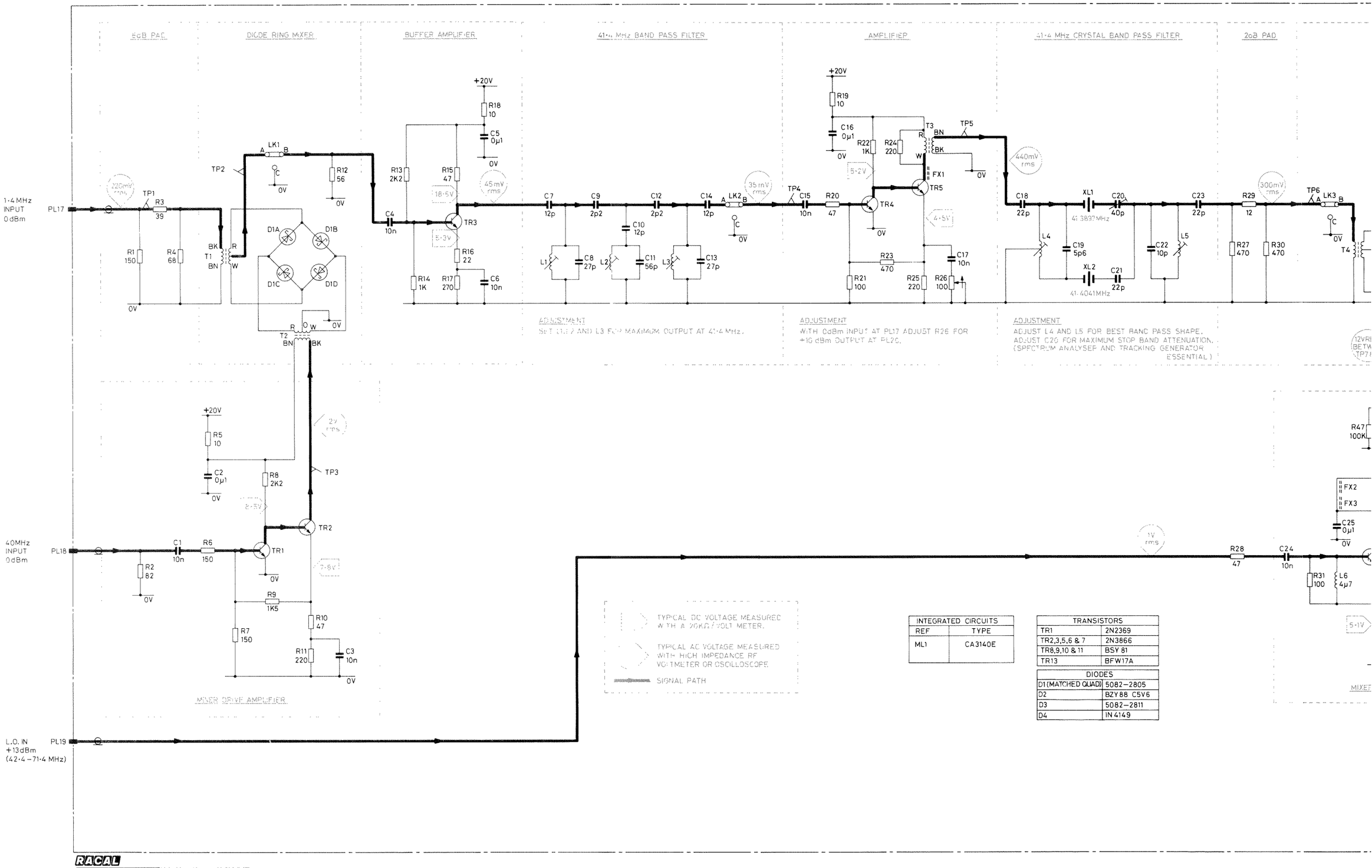
L1		Coil Assembly			AT82389
L2		Coil Assembly			AT82388
L3		Coil Assembly			AT82389
L4		Coil Assembly			AT82391
L5		Coil Assembly			AT82390
L6	4µ7H	Choke		10	939887
L7	4µ7H	Choke		10	939887
L8		Coil Assembly			AT82395
L9		Coil Assembly			AT82392
L10		Coil Assembly			AT82393
L11		Coil Assembly			AT82394
L12	1µ0H	Choke		10	938966
L13	1µ0H	Choke		10	938966

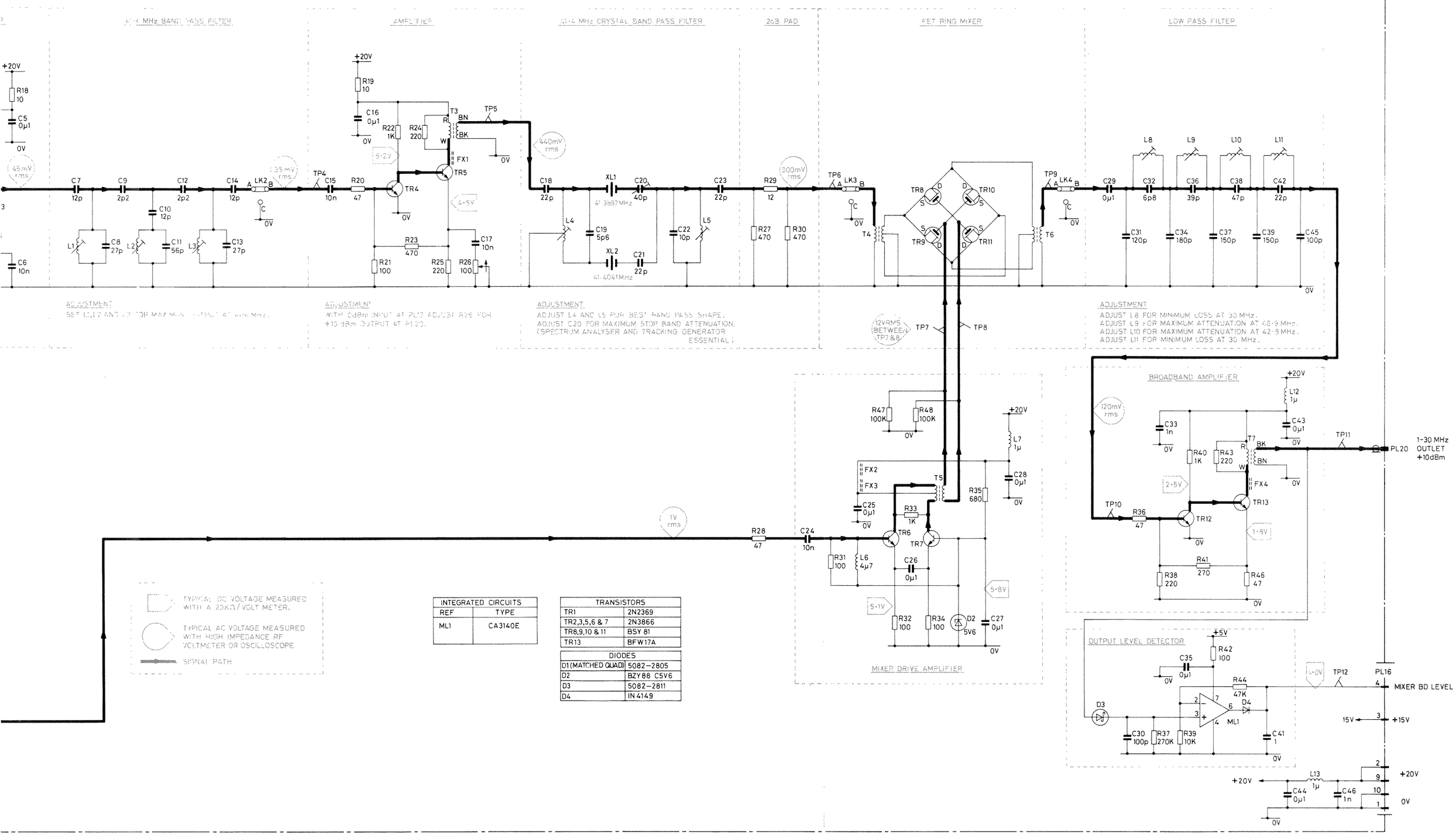
Transformers

T1		Transformer Assembly			AT82396
T2		Transformer Assembly			AT82397
T3		Transformer Assembly			AT82398
T4		Transformer Assembly			AT82401
T5		Transformer Assembly			AT82400
T6		Transformer Assembly			AT82399
T7		Transformer Assembly			AT82402

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Connectors					
PL16		Plug, 10 way			939968
PL17		Plug, coaxial, 50 ohms			935268
PL18		Plug, coaxial, 50 ohms			935268
PL19		Plug, coaxial, 50 ohms			935268
PL20		Plug, coaxial, 50 ohms			935268
Diodes					
D1		Schottky, matched quad, 5082-2805			916623
D2		Zener, 5.6 V, 400 mW, BZX79C5V6			921749
D3		Schottky 5082-2811			919460
D4		Silicon 1N4149			923222
Transistors					
TR1		NPN Silicon 2N2369			906842
TR2		NPN Silicon 2N3866			917219
TR3		NPN Silicon 2N3866			917219
TR4		NPN Silicon BFX89			916627
TR5		NPN Silicon 2N3866			917219
TR6		NPN Silicon 2N3866			917219
TR7		NPN Silicon 2N3866			917219
TR8		N-channel MOSFET BSV81			918424
TR9		N-channel MOSFET BSV81			918424
TR10		N-channel MOSFET BSV81			918424
TR11		N-channel MOSFET BSV81			918424
TR12		NPN Silicon BFX89			916627
TR13		NPN Silicon BFW17A			920012
Integrated Circuits					
ML1		Operational Amplifier CA3140E			932204

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Crystals					
XL1		Quartz 41.3897 MHz			AD82425
XL2		Quartz 41.4014 MHz			AD82426
Miscellaneous					
LK1-LK4		Link, shorting			927090
FX1-FX4		Ferrite Bead FX1115			900461
		Test Point			936148
		Captive Fastener			930396
		8-pin DIL IC socket			940901
		Heatsink (TR2, 3, 5, 13)			919967
		Heatsink (TR6, 7)			905416


1·4 MHz INPUT 0 dBm
PL17
220mV rms
TP1
R3 39
R1 150
R4 68
0V
BK
R
T1
BN
W
TP2
LK1
A
B
C
0V
R12 56
0V
D1A
D1B
D1C
D1D
T2
BN
BK
R
O
W
0V
EdB PAD
DIODE RING MIXER
+20V
R18 10
C5 0µ1
0V
R13 2K2
R15 47
18·6V
45 mV rms
C4 10n
TR3
5·3V
R16 22
R14 1K
R17 270
C6 10n
BUFFER AMPLIFIER
C7 12p
C9 2p2
C12 2p2
C14 12p
A
LK2
B
C
0V
L1
C8 27p
L2
C10 12p
C11 56p
L3
C13 27p
35 mV rms
41·4 MHz BAND PASS FILTER
ADJUSTMENT
SET L1, 2 AND L3 FOR MAXIMUM OUTPUT AT 41·4 MHz.
+20V
R19 10
C16 0µ1
0V
R22 1K
R24 220
T3
R
W
BN
BK
TP5
0V
5·2V
FX1
TR5
TR4
4·5V
TP4
C15 10n
R20 47
0V
R23 470
R21 100
R25 220
R26 100
C17 10n
AMPLIFIER
ADJUSTMENT
WITH 0dBm INPUT AT PL17 ADJUST R26 FOR
+10 dBm OUTPUT AT PL20.
440mV rms
C18 22p
XL1
41·3837MHz
C20 40p
C23 22p
L4
C19 5p6
XL2
41·4041MHz
C21 22p
C22 10p
L5
41·4 MHz CRYSTAL BAND PASS FILTER
ADJUSTMENT
ADJUST L4 AND L5 FOR BEST BAND PASS SHAPE.
ADJUST C20 FOR MAXIMUM STOP BAND ATTENUATION.
(SPECTRUM ANALYSER AND TRACKING GENERATOR
ESSENTIAL)
300mV rms
R29 12
R27 470
R30 470
TP6
A
LK3
B
C
0V
T4
2dB PAD
12VRI
(BETW
TP7
+20V
R5 10
C2 0µ1
0V
2V rms
TP3
R8 2K2
8·5V
TR2
TR1
0V
7·8V
R9 1K5
R10 47
R7 150
R11 220
C3 10n
0V
R2 82
0V
C1 10n
R6 150
MIXER DRIVE AMPLIFIER
40MHz INPUT 0dBm
PL18
L.O. IN +13dBm (42·4 – 71·4 MHz)
PL19
1V rms
R28 47
C24 10n
R31 100
L6 4µ7
FX2
FX3
C25 0µ1
0V
5·1V
R47 100K
MIXER
TYPICAL DC VOLTAGE MEASURED WITH A 20KΩ/VOLT METER.
TYPICAL AC VOLTAGE MEASURED WITH HIGH IMPEDANCE RF VOLTMETER OR OSCILLOSCOPE
SIGNAL PATH
INTEGRATED CIRCUITS
REF
TYPE
ML1
CA3140E
TRANSISTORS
TR1 2N2369
TR2,3,5,6 & 7 2N3866
TR8,9,10 & 11 BSY 81
TR13 BFW17A
DIODES
D1 (MATCHED QUAD) 5082–2805
D2 BZY88 C5V6
D3 5082–2811
D4 1N4149
RACAL
TH 3071 DC81651 9.1
2 1/2

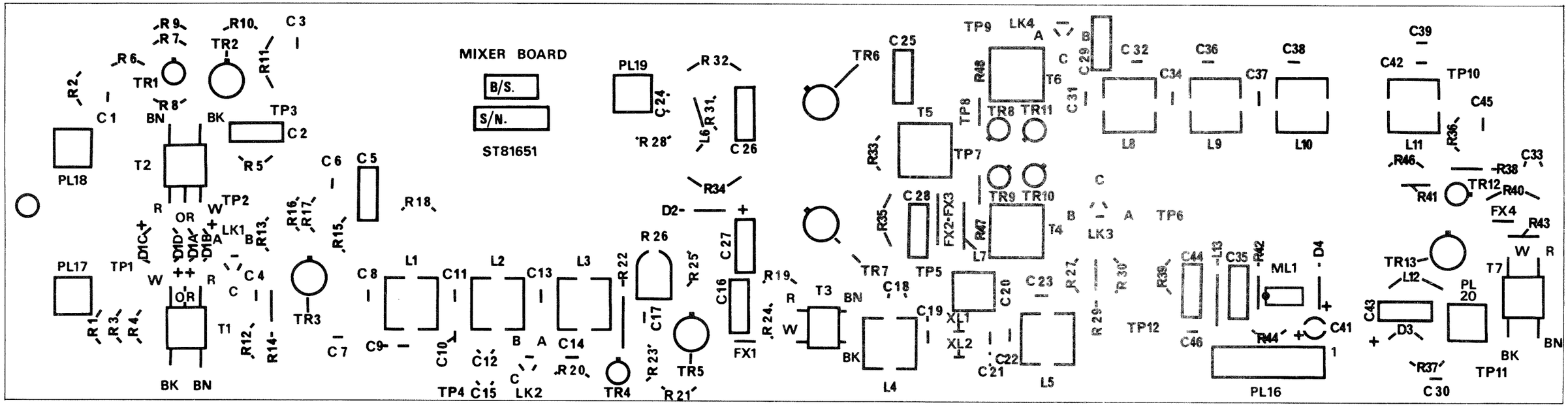


INTEGRATED CIRCUITS	
REF	TYPE
ML1	CA3140E

TRANSISTORS	
TR1	2N2369
TR2,3,5,6 & 7	2N3866
TR8,9,10 & 11	BSY 81
TR13	BFW17A

DIODES	
D1 (MATCHED QUAD)	5082–2805
D2	BZY88 C5V6
D3	5082–2811
D4	IN 4149

Circuit : Mixer Board Fig. 9.1



RACAL

TH3071	DA81650/4
1	

Layout : Mixer Board

Fig. 9·2

CHAPTER 10

MODULATION BOARD

CONTENTS

Tables

Illustrations

CHAPTER 10

MODULATION BOARD

INTRODUCTION

1. The modulation board accepts the line 1 and 2 audio signals applied to the rear panel, microphone inputs from the front panel, and the 1.4 MHz signal from the reference generator board. C-MOS analogue switches are used to route the incoming audio signals to the USB and/or the LSB balanced modulators which mix the selected audio signals with the 1.4 MHz signal to produce double sideband suppressed carrier signals. The wanted sidebands are selected using 1.4 MHz crystal filters, and the two sidebands are applied, together with a 1.4 MHz re-inserted carrier, to a summing output amplifier.

FUNCTIONAL DESCRIPTION

2. The following functional description paragraphs should be read in conjunction with the simplified block diagram of the modulation board given in Fig. 10.1 (at the end of the chapter).

Line Input Amplifiers

3. The audio line 1 and line 2 signals applied to the rear panel are routed via isolation transformers and the line level potentiometers to the line 1 and line 2 input amplifiers respectively. The fixed-level signals from front-panel connected carbon microphones are also routed to these input amplifiers, whilst the nominal 800 Hz output signal from the sidetone oscillator is applied only on selection of a built-in test routine. The output signals from the line 1 and line 2 input amplifiers, together with the TSK signals from the optional FSK board, are applied to C-MOS analogue switches for application to the appropriate sideband circuitry, dependent on the mode selected (para. 6).

Monitor Amplifiers

4. The output signals from the line 1 and line 2 monitor amplifiers are taken to the front-panel mounted LINE sockets where they can be monitored using suitable headphones. The signal available at each line socket is dependent upon the selected mode, as given in Table 1.

Table 1: Monitor Signals

MODE SELECTED	MONITOR SIGNAL	
	LINE 1	LINE 2
USB	LINE 1 AUDIO	-
LSB	LINE 1 AUDIO	-
AM	LINE 1 AUDIO	-
CW	KEYED SIDETONE	-
FSK	TSK	-
ISB 1	LINE 1 AUDIO	LINE 2 AUDIO
ISB 2	LINE 1 AUDIO + TSK	-
ISB 3	TSK	LINE 2 AUDIO

Voice Operated Transmission (VOX)

5. When VOX is selected at the front panel, in conjunction with the appropriate mode (CW or any mode that uses the line 1 input amplifier), the muting of the RF output signal (from the RF output board) is governed by the presence or absence of the line 1 audio signal or the audio sidetone signal (CW mode) applied to the VOX circuit. The fast attack/slow decay characteristic of this circuit removes the mute condition as soon as the presence of an audio input signal is detected, and re-applies the mute condition approximately one second after the audio input signal disappears.

Audio Signal Switching

6. The C-MOS analogue switches route the TSK, line 1 and line 2 audio signals to the appropriate sideband circuit dependent upon the selected mode, as given in Table 2.

Table 2: Audio Signal Switching

MODE SELECTED	USB CHANNEL	LSB CHANNEL
USB	LINE 1 AUDIO	-
LSB	-	LINE 1 AUDIO
AM	LINE 1 AUDIO	-
CW	-	-
FSK	TSK	-
ISB 1	LINE 1 AUDIO	LINE 2 AUDIO
ISB 2	LINE 1 AUDIO	TSK
ISB 3	TSK	LINE 2 AUDIO

Balanced Modulators

7. Since the operation of the upper sideband circuit is essentially the same as that of the lower sideband circuit, only the former is described. The selected audio signal is applied to a level control stage, either direct (AGC OFF) or via a gain controlled amplifier (AGC ON). The level control

stage reduces the sideband level by 6 dB for the ISB and AM modes to maintain the correct peak envelope power, and is also used to mute the sideband when it is not selected. This circuit is further used to provide a 2 dB reduction in sideband level when a pilot carrier between -10 dB and -20 dB is selected. The balanced modulator mixes the audio signal with an amplified 1.4 MHz signal to produce a double sideband suppressed carrier signal. The wanted sideband is then selected using a crystal bandpass filter (note that to compensate for sideband inversion which occurs on the mixer board, the USB filter has LSB characteristics and the LSB filter has USB characteristics).

8. The output signal from the crystal filter is amplified before application to a summing amplifier, and also to a level detector which forms part of the AGC circuit for the input amplifier stage. When AGC is selected, the peak envelope power of the sideband is maintained at a constant level for changes in audio input of up to plus or minus 10 dB.

Summing Amplifier

9. The two sidebands are combined, along with a re-inserted 1.4 MHz carrier, in a summing amplifier. The gain of this stage is reduced by a preset amount when LOW POWER is selected. The level of the re-inserted carrier is adjusted via a control loop which uses the output voltage of the processor-controlled digital to analogue converter (DAC). For CW operation, the key input is fed via a shaping circuit to the carrier level control ciruit to provide ON-OFF keying.

Metering

10. An 8-channel multiplexer is included on the modulation board (not shown in Fig. 10.1) for metering of the audio line input levels, sideband output signal levels and sideband AGC voltage levels.

CIRCUIT DESCRIPTION (Figs. 10.2 and 10.3)

Line 1 and Line 2 Input Amplifiers

11. These two audio amplifiers both use one section of a quad operational amplifier, ML3a and ML6a. As the operation is the same for both input amplifiers, the line 1 amplifier only is described.

12. ML3a is connected as an inverting summing amplifier, where the values of the input resistors R1, R2, R15 are scaled to provide, in conjunction with feedback resistor R16, the required gain characteristics. The non-inverting input is taken to +5 V (via R4) so that the amplified audio output signal is effectively superimposed on a 5 V d.c. level. This is necessary to satisfy the switching requirements of the C-MOS multiplexer device ML5 and also the C-MOS analogue switches ML2a, ML2b; these devices require that the level of a signal to be switched is between certain prescribed levels which are related to VDD and VSS.

13. A potential divider, R10 to R13, together with diodes D1 to D4, is used to introduce clipping at the output of each input amplifier for signals outside the range 5 V plus and minus 2 V.

Line 1 and Line 2 Monitor Amplifiers

14. The two line monitor amplifiers, ML3b and ML6b, are both connected as inverting summing amplifiers. The four input lines taken to the line 1 monitor amplifier are from the line 1 input amplifier ML3a, the TSK input amplifier ML17a, the Rx audio 1 line (from an associated receiver) and the audio sidetone oscillator (para. 39), whilst the line 2 monitor amplifier receives inputs from the line 2 input amplifier and the Rx Audio 2 line only. The preset resistors R29 and R30 provide for gain adjustment, and the output signals are taken to the front-panel LINE 1 and LINE 2 sockets.

Audio Signal Routeing

15. The interface between the modulation board and the processor board comprises the DB0 to DB7 data bus (PL12 pins 10 to 17), and three output data strobes OP2A, OP2B, OP2C, from the front panel interface board (Chap. 5), at PL12 pins 20, 19 and 18 respectively. The strobe and data bus input lines are applied to three quad low-to-high voltage level shifters ML26, ML27, ML28, to convert 5 V TTL-level signals to 12 V C-MOS-level signals. Output strobe 2 C is used to clock metering select data into quad latch ML19 (para. 24), output strobe 2B is used to clock miscellaneous control data into quad latches ML22, ML29 (Fig. 10.3), whilst output strobe 2A is used to clock audio routeing, audio attenuation and AGC selection data into quad latches ML20, ML21, as given in Tables 3, 4 and 5.

Table 3: Port 2A Data

DATA BUS	FUNCTION
0	Analogue Switch Control lines Table 4
1	
2	USB select without AGC
3	USB select with AGC
4	LSB select without AGC
5	LSB select with AGC
6	Audio Attenuation Table 5
7	

Table 4: Analogue Switching Data

DATA BUS		SIDEBAND		MODE
1	0	UPPER	LOWER	
0	0	LINE 1	LINE 2	USB, AM, ISB1 (USB + LSB)
0	1	LINE 2	LINE 1	LSB
1	0	TSK	LINE 2	FSK, ISB3 (LSB + FSK)
1	1	LINE 1	TSK	ISB2 (USB + FSK)

Table 5: Audio Attenuation

DATA BUS		ATTENUATION	MODE
7	6		
0	0	0 dB	USB, LSB, FSK
0	1	-2 dB	PILOT -10 to -20
1	0	-6 dB	AM, ISB
1	1	-7 dB	ISB + PILOT -10 to -20

16. The analogue switching data (Table 4) is applied to the A and B control inputs of a differential 4-channel multiplexer ML5. The two binary control inputs select one of four pairs of channels and route the selected X and Y input signals to the X and Y output pins.

AGC ON/OFF Select

17. The AGC select switches SA, SB, are connected via PL12 pins 31 and 32 to the front panel interface board (together with the VOX output at PL12 pin 23 - see para. 21) where the state of each switch (0V for AGC ON, +5 V from pull-up resistor on front panel interface board for AGC OFF) is monitored by the processor. The AGC select information for each sideband is then conveyed, together with mode select data, via data bus lines DB2 to DB5 (Table 3), and thence via latches ML20 and ML21 to enable the appropriate analogue switches (ML2a, ML2b or neither for USB, ML17a, ML17b or neither for LSB). Note that AGC is always de-selected in the appropriate audio path when FSK is selected.

Audio Attenuation

18. The USB and LSB level selector circuits (ML2, ML3c, ML3d and ML7, ML6c, ML6d) automatically introduce the required amount of audio attenuation for the selected mode (Table 5), and at the same time, the required level of AGC voltage applied to the USB and LSB gain controlled amplifiers (ML4, ML8) is automatically selected by ML16a and ML16b.

AGC Stages

19. When selected, the AGC circuit controls the gain of the audio amplifier in order to maintain the peak envelope power of the sideband at a constant level for changes in the audio input level of up to plus and minus 10 dB. As the circuit for each sideband is similar, only that for the upper sideband is described, as follows.

20. The USB level detector TR10, ML18a, TR12 (Fig. 10.3) is an RF level peak detector. The d.c. output voltage from TR12, on which is superimposed any audio modulation, is applied to an audio peak detector stage ML17b, D5 (Fig. 10.2), which feeds integrator stage ML17c followed by inverting d.c. amplifier stage ML17d. The output voltage level from ML17d is then used to control the gain of the USB audio amplifier stage ML4, where stage gain is controlled by the level of the applied AGC voltage (an increase in AGC voltage reduces the stage gain).

VOX Control

21. The VOX control circuit comprises ML15a, ML15b, TR1, ML23a and TR2. The output signal from the line 1 input amplifier stage ML3a is applied via C27 to non-inverting amplifier stage, ML15a which feeds voltage comparator stage ML15b. Whilst the level of the audio signal applied to the non-inverting input of ML15a is above the threshold level set by R69, then the output from ML15b repeatedly triggers monostable ML23a. The resulting '1' at the Q output of ML23a results in a '0' at the output of TR2, and this is routed to the processor board via the front panel interface board to signify the presence of the audio signal.

22. When a break in the audio signal occurs which is greater than the period of the monostable (approximately 700 milliseconds), the output from TR2 is pulled up to +5 V (by a pull-up resistor on the front panel interface board) and the processor causes the mute condition to be applied to the RF output board.

23. The operation of the circuit when an audio sidetone signal is present is similar except that the trigger signal for the monostable is provided by TR1.

Metering Selector

24. An eight-channel multiplexer device ML24 routes one of seven analogue signals applied to the Y input pins (the Y7 input is not used) to the Y output pin, as selected by the binary levels at the A, B and C input pins (Table 6). These levels, which are clocked into quad latch ML19 by the application of output strobe OP2C (para. 15), are governed by the information from the front panel SET/RF/LINE switch which is routed to the processor via the front panel interface board.

Table 6: Metering Selector

DATA BUS			ML 24 INPUT SELECTED	METERED SIGNAL	METERING MODE
7	6	5			
0	0	0	Y0	USB PEAK RF	SET 1 (NO AGC)
0	0	1	Y1	USB AGC	SET 1 (AGC)
0	1	0	Y2	LSB AGC	SET 2 (AGC)
0	1	1	Y3	LINE 1 AUDIO	LINE 1
1	0	0	Y4	LINE 2 AUDIO	LINE 2
1	0	1	Y5	LSB PEAK RF	SET 2 (NO AGC)
1	1	0	Y6	BOARD O/P LEVEL	SELF TEST

25. The Y output signal from ML24 is taken direct to an analogue multiplexer stage on the front panel interface board for d.c. signals, and via peak detector stage ML14, D9, for audio signals.

Balanced Modulators

26. The USB and LSB balanced modulator circuits are given, one above the other, in Fig. 10.3. As the operation is the same for both sidebands, that for the upper sideband only is described, as follows:

27. The 1.4 MHz signal from the reference generator board is applied to mixer drive amplifier TR3 which provides the relatively higher switching input for the balanced modulator T1, ML10, T3. The USB audio signal input is applied to transformer T1 via R95, C54 and C57, and transformer T3 couples the output to amplifier stage TR5. This is followed by the 1.4 MHz USB crystal filter and a further amplifier stage TR8, which is only enabled when USB is selected. Note that due to a frequency inversion which takes place on the mixer board, the 1.4 MHz USB filter has LSB characteristics, and the 1.4 MHz LSB filter has USB characteristics.

Gain-Controlled 1.4 MHz Carrier Amplifier

28. The 1.4 MHz input at PL15 is coupled by C52 to a gain-controlled amplifier stage ML1a, ML1b and ML11a. The gain control voltage is applied to the non-inverting input of ML11a, which in turn controls the current source transistor ML1b. ML1 is a 14-pin DIL integrated circuit containing five general-purpose silicon NPN transistors where two are internally connected to form a differential pair (ML1a).

Carrier Level Control

29. A simplified diagram of the carrier level control circuitry is given in Fig. 10(a). The digital-to-analogue converter on the front panel interface board is used, in conjunction with a voltage comparator and a software successive approximation routine, for analogue metering purposes. Approximately once every 20 milliseconds however, and also when metering is not taking place, the digital-to-analogue converter is used to route a carrier level control voltage via sample-and-hold switch ML12a to hold-capacitor C72. This voltage is produced under software control where the level of the voltage is dependent on the selected mode.

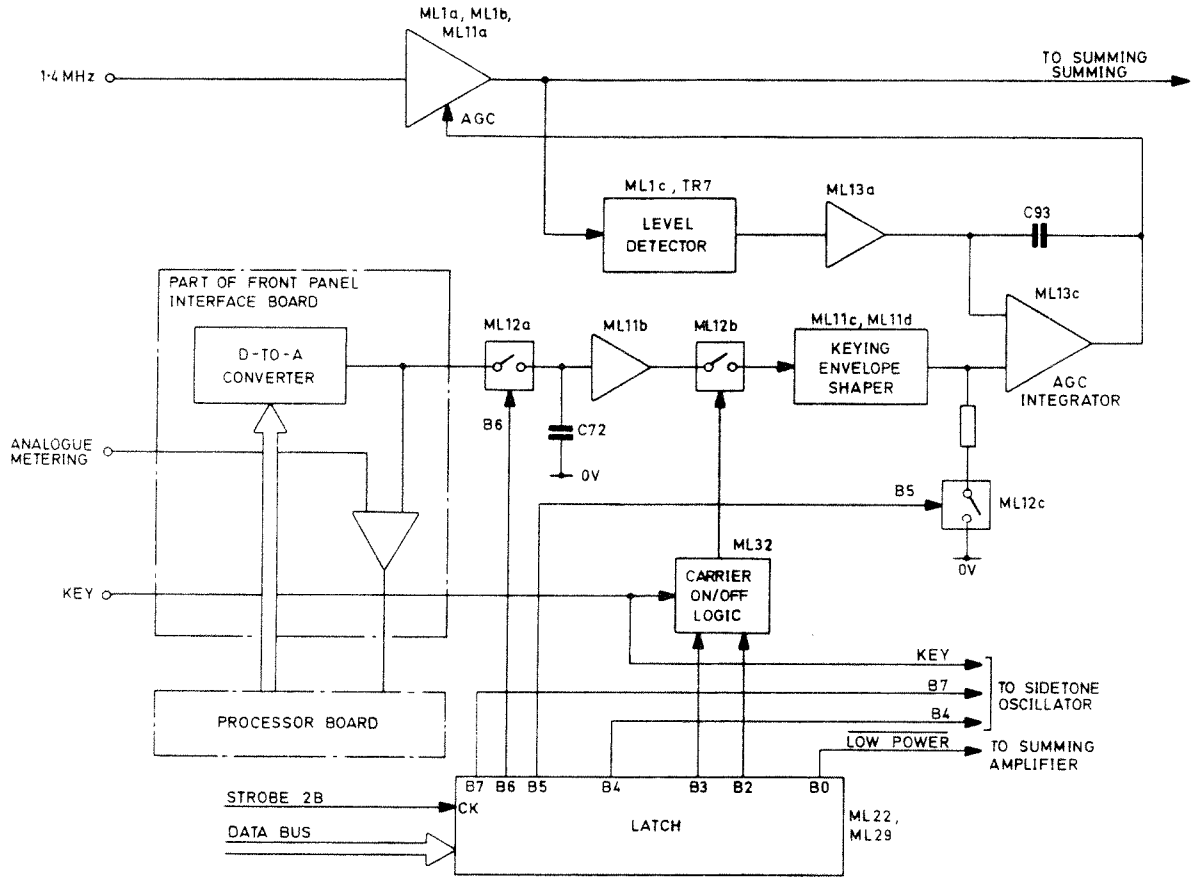


Fig. 10 (a) Simplified Diagram : Carrier Level Control

30. The carrier ON/OFF logic circuit (ML32) and the analogue switches (ML12, ML16) are also under control of the processor, and respond to output strobe 2B which is applied to the clock inputs of latches ML22 and ML29 (Table 7).

Table 7: Carrier Level Control (Port 2B)

DATA BUS	FUNCTION
0	$\overline{\text{LOW POWER}}$
1	NOT USED
2	KEY ENABLE
3	$\overline{\text{CARRIER ENABLE}}$
4	SIDETONE ENABLE
5	LOW/$\overline{\text{HIGH}}$ RANGE
6	DAC SAMPLE
7	TEST TONE ENABLE

Low Power

31. When a '0' is present at the Q1 output of ML22 (Fig. 10.3), TR16 is held off and the output level of the summing amplifier is set by preset resistor R165.

Key Enable

32. The key enable line (Q3 output of latch ML22) is set to a '1' to enable open-collector NAND gate ML32b for the key input at PL12 pin 25.

Carrier Enable

33. The carrier $\overline{\text{enable}}$ line (Q4 output of ML22) is used in conjunction with the key enable line to control the carrier ON/OFF switch ML12b. When enabled, ML12b routes the sample-and-hold voltage stored in C72 to the AGC integrator stage ML13c (via the keying envelope shaper), and this in turn controls the level of the re-inserted 1.4 MHz carrier. Table 8 shows the carrier state for the applicable control conditions.

Table 8: Carrier ON/OFF Switching

KEY STATE	KEY ENABLE	$\overline{\text{CARRIER ENABLE}}$	CARRIER STATE
X	0	0	ON
DOWN	1	0	ON
UP	1	0	OFF
X	X	1	OFF

X denotes either condition

Carrier Level Detector

34. This stage, which comprises differential transistor-pair ML1c and TR7, produces a d.c. output voltage, the level of which in proportional to the peak level of the 1.4 MHz output signal from ML1a. The output from TR7 is buffered by voltage-follower ML13a, and is then applied to the AGC integrator ML13c.

Keying Envelope Shaper

35. The keying envelope shaper comprises an active low-pass filter M111c, ML11d. It modifies the waveshape of the applied keying square wave from ML12b to produce a keyed carrier signal which complies with CCIR Recommendation 328-4 at a keying rate of 25 words per minute. Fig. 10(b) shows the relevant wave shapes.

36. The output signal from ML11d is applied to the non-inverting input of the AGC integrator ML13c via R158. For carrier levels in the range -15 dB to -30 dB, a '1' is applied to analogue switch ML12c; the switch closes, R162 is connected to 0V to form a potential divider, and the carrier level voltage from the processor is scaled accordingly. This circuit is included to produce a linear control characteristic over the range 0 dB to -30 dB.

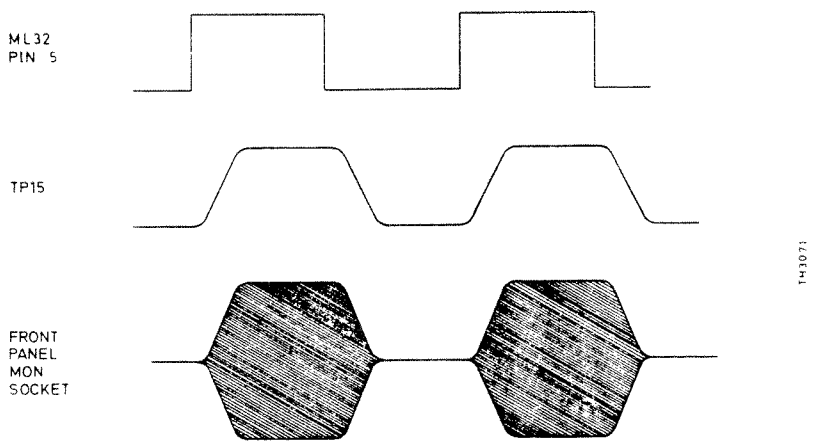


Fig. 10(b) Envelope Waveforms

AGC Integrator

37. The AGC integrator ML13c, C93, controls the gain of the 1.4 MHz amplifier via ML11a, by controlling the current source transistor ML1b. The loop stabilises when the output from the carrier level detector (at TP8) is equal to the voltage applied to the non-inverting input of the AGC detector (at TP15). Thus whilst a carrier is present, the negative voltage at the inverting input of ML11a is equal to the negative voltage at the non-inverting input, and since this voltage is less negative than -12 V, a positive voltage is present at the output of comparator ML13b (inverting input held at just less negative than -12 V); due to the presence of D12 however, this positive output voltage has no effect.

38. When the carrier is switched off, the voltage at TP15 falls to zero, and the output of the AGC integrator ramps down towards -15 V. When however, the gain of the 1.4 MHz amplifier falls to the point when the voltage level at the inverting input of ML11a is at -12 V, the comparator stage ML13b changes state, the output switches from +15 V to -15 V, current is drawn from the AGC integrator, and the loop stabilises with approximately -12V at the non-inverting input of ML11a. This holds the 1.4 MHz carrier amplifier in the 'just-off' condition and so prevents the introduction of a hysteresis effect when the amplifier is again turned on.

Sidetone Oscillator

39. ML31 is a multivibrator connected in the astable (free-running) mode. When enabled, it produces a 12 V peak-to-peak output signal at approxmiately 800 Hz (timing components R181, C103), which is routed as a sidetone signal to the line 1 monitor amplifier ML3b (Fig. 10.2), and to TR1 which forms part of the VOX circuitry (also on Fig. 10.2). It is also applied to the line 1 and line 2 input amplifiers as a test tone during one of the built-in self-test routines.

40. The oscillator is controlled by the Q1(B4) and Q4(B7) outputs of latch ML29 (Table 7), and by the output from the carrier ON/OFF logic ML32. Under normal operating conditions, the sidetone output is only produced when a carrier is present ('1' at the control input of ML12d to remove the reset condition from ML31) and when a '1' is present at the Q1 output of latch ML29 (routed to the astable input of ML31). For test purposes, a '1' is required at the Q4 output of ML29 in place of a '1' output from ML32; this is routed to ML16c to remove the reset condition from ML31, and is also applied to ML16d to route the test tone to the input amplifiers.

Summing Amplifier

41. The two sideband signals are combined, together with a re-inserted carrier, in a summing amplifier, TR14 and TR15. C106 and diodes D14, D15 and D16 are included for surge limiting purposes. The 1.4 MHz output signal is taken from a low impedance tap on transformer T5 and is applied via C97 and coaxial connector PL14 to the mixer board (chap. 9). The output from the peak level detector TR17, D13, ML14b, is applied to the metering multiplexer stage ML24 (Fig. 10.2), described in para. 24, and is used for self-test purposes.

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
		MODULATION BOARD (ST81649)			
Resistors					
R1	47k	Metal Oxide		2	913496
R2	1k	Metal Oxide		2	913489
R3	1k	Metal Oxide		2	913489
R4	33k	Metal Oxide		2	913495
R5	2k2	Metal Oxide		2	916546
R6	47k	Metal Oxide		2	913496
R7	1k	Metal Oxide		2	913489
R8	1k	Metal Oxide		2	913489
R9	33k	Metal Oxide		2	913495
R10	2k2	Metal Oxide		2	916546
R11	820	Metal Oxide		2	917065
R12	560	Metal Oxide		2	917061
R13	820	Metal Oxide		2	917065
R14	47k	Metal Oxide		2	913496
R15	82k	Metal Oxide		2	915189
R16	33k	Metal Oxide		2	913495
R17	82k	Metal Oxide		2	915189
R18	33k	Metal Oxide		2	913495
R19	2k7	Metal Oxide		2	916548
R20	2k7	Metal Oxide		2	916548
R21	560	Metal Oxide		2	917061
R22	560	Metal Oxide		2	917061
R23	1k8	Metal Oxide		2	911148
R24	2k7	Metal Oxide		2	916548
R25	5k6	Metal Oxide		2	918128
R26	5k6	Metal Oxide		2	918128
R27	2k7	Metal Oxide		2	916548
R28	5k6	Metal Oxide		2	918128
R29	22k	Variable, Preset		20	920314
R30	22k	Variable, Preset		20	920314
R31	8k2	Metal Oxide		2	918202
R32	560	Metal Oxide		2	917061
R33	560	Metal Oxide		2	917061
R34	8k2	Metal Oxide		2	918202
R35	22k	Metal Oxide		2	913493

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Resistors (cont'd)					
R36	3k9	Metal Oxide		2	915074
R37	12k	Metal Oxide		2	917952
R38	3k3	Metal Oxide		2	910111
R39	220k	Metal Oxide		2	921771
R40	220k	Metal Oxide		2	921771
R41	1k2	Metal Oxide		2	911179
R42	1k2	Metal Oxide		2	911179
R43	3k9	Metal Oxide		2	915074
R44	1k8	Metal Oxide		2	911148
R45	3k9	Metal Oxide		2	915074
R46	1k8	Metal Oxide		2	911148
R47	4k7	Variable, Preset		20	920311
R48	100k	Metal Oxide		2	915190
R49	100k	Metal Oxide		2	915190
R50	4k7	Variable, Preset		20	920311
R51	10k	Metal Oxide		2	914042
R52	10k	Metal Oxide		2	914042
R53	10k	Metal Oxide		2	914042
R54	22k	Variable, Preset		20	920314
R55	10k	Metal Oxide		2	914042
R56	22k	Variable, Preset		20	920314
R57	22k	Metal Oxide		2	913493
R58	22k	Metal Oxide		2	913493
R59	8k2	Metal Oxide		2	918202
R60	8k2	Metal Oxide		2	918202
R61	2k2	Metal Oxide		2	916546
R62	2k2	Metal Oxide		2	916546
R63	2k2	Metal Oxide		2	916546
R64	2k2	Metal Oxide		2	916546
R65	56k	Metal Oxide		2	913497
R66	56k	Metal Oxide		2	913497
R67	100k	Metal Oxide		2	915190
R68	470	Metal Oxide		2	920758
R69	47k	Metal Oxide		2	913496
R70	47k	Metal Oxide		2	913496
R71	33k	Metal Oxide		2	913495
R72	3k9	Metal Oxide		2	915074
R73	10k	Metal Oxide		2	914042
R74	10k	Metal Oxide		2	914042
R75	22k	Metal Oxide		2	913493

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Resistors (cont'd)					
R76	22k	Metal Oxide		2	913493
R77	220k	Metal Oxide		2	921771
R78	100k	Metal Oxide		2	915190
R79	12k	Metal Oxide		2	917952
R80	120k	Metal Oxide		2	915373
R81	22k	Metal Oxide		2	913493
R82	100	Metal Oxide		2	910388
R83	220	Metal Oxide		2	910390
R84	4k7	Metal Oxide		2	913490
R85	2k2	Metal Oxide		2	916546
R86	220	Metal Oxide		2	910390
R87	4k7	Metal Oxide		2	913490
R88	2k2	Metal Oxide		2	916546
R89	56	Metal Oxide		2	917055
R90	100	Metal Oxide		2	910388
R91	100	Metal Oxide		2	910388
R92	100	Metal Oxide		2	910388
R93	33	Metal Oxide		2	917060
R94	100	Metal Oxide		2	910388
R95	330	Metal Oxide		2	915690
R96	100	Metal Oxide		2	910388
R97	330	Metal Oxide		2	915690
R98	560	Metal Oxide		2	917061
R99	5k6	Metal Oxide		2	918128
R100	10k	Metal Oxide		2	914042
R101	4k7	Metal Oxide		2	913490
R102	10k	Metal Oxide		2	914042
R103	10k	Metal Oxide		2	914042
R104	47k	Metal Oxide		2	913496
R105	1k	Metal Oxide		2	913489
R106	1k8	Metal Oxide		2	911148
R107	15k	Metal Oxide		2	920645
R108	10k	Metal Oxide		2	914042
R109	6k8	Metal Oxide		2	910112
R110	1k8	Metal Oxide		2	911148
R111	6k8	Metal Oxide		2	910112
R112	1k8	Metal Oxide		2	911148
R113	47	Metal Oxide		2	917063
R114	1k	Metal Oxide		2	913489
R115	330	Metal Oxide		2	915690

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Resistors (cont'd)					
R116	47	Metal Oxide		2	917063
R117	1k	Metal Oxide		2	913489
R118	330	Metal Oxide		2	915690
R119	6k8	Metal Oxide		2	910112
R120	1k	Metal Oxide		2	913489
R121	1k	Metal Oxide		2	913489
R122	6k8	Metal Oxide		2	910112
R123	1k	Metal Oxide		2	913489
R124	6k8	Metal Oxide		2	910112
R125	1k	Metal Oxide		2	913489
R126	1k2	Metal Oxide		2	911179
R127	1k2	Metal Oxide		2	911179
R128	47	Metal Oxide		2	917063
R129	1k8	Metal Oxide		2	911148
R130	330	Metal Oxide		2	915690
R131	47	Metal Oxide		2	917063
R132	1k8	Metal Oxide		2	911148
R133	330	Metal Oxide		2	915690
R134	2k2	Metal Oxide		2	916546
R135	1k5	Metal Oxide		2	911166
R136	1k5	Metal Oxide		2	911166
R137	10k	Metal Oxide		2	914042
R138	1k	Metal Oxide		2	913489
R139	1k	Metal Oxide		2	913489
R140	39k	Metal Oxide		2	900993
R141	1k8	Metal Oxide		2	911148
R142	1k8	Metal Oxide		2	911148
R143	15k	Metal Oxide		2	920645
R144	15k	Metal Oxide		2	920645
R145	39k	Metal Oxide		2	900993
R146	22k	Metal Oxide		2	913493
R147	82	Metal Oxide		2	917057
R148	4k7	Metal Oxide		2	913490
R149	1k	Metal Oxide		2	913489
R150	4k7	Metal Oxide		2	913490
R151	1k	Metal Oxide		2	913489
R152	1k	Metal Oxide		2	913489
R153	47	Metal Oxide		2	917063
R154	22k	Metal Oxide		2	913493
R155	100k	Metal Oxide		2	915190

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Resistors (cont'd)					
R156	22k	Metal Oxide		2	913493
R157	10k	Metal Oxide		2	914042
R158	47k	Metal Oxide		2	913496
R159	10k	Variable, Preset		20	920312
R160	10k	Variable, Preset		20	920312
R161	47k	Variable, Preset		20	920313
R162	10k	Metal Oxide		2	914042
R163	1k5	Metal Oxide		2	911166
R164	470	Metal Oxide		2	920758
R165	10k	Variable, Preset		20	920312
R166	1k5	Metal Oxide		2	911166
R167	1k5	Metal Oxide		2	911166
R168	180	Metal Oxide		2	915465
R169	82	Metal Oxide		2	917057
R170	22k	Metal Oxide		2	913493
R171	47	Metal Oxide		2	917063
R172	39k	Metal Oxide		2	900993
R173	5k6	Metal Oxide		2	918128
R174	2k2	Metal Oxide		2	916546
R175	390	Metal Oxide		2	916331
R176	22k	Metal Oxide		2	913493
R177	27k	Metal Oxide		2	913494
R178	270k	Metal Oxide		2	923598
R179	56k	Metal Oxide		2	913497
R180	12k	Metal Oxide		2	917952
R181	12k	Metal Oxide		2	917952
R182	22k	Metal Oxide		2	913493
R183	10k	Metal Oxide		2	914042
R184	1k	Metal Oxide		2	913489
Capacitors			Volts		
C1	6µ8	Tantalum Bead	35	20	923573
C2	6µ8	Tantalum Bead	35	20	923573
C3	6µ8	Tantalum Bead	35	20	923573
C4	1µ0	Tantalum Bead	35	20	923571
C5	6µ8	Tantalum Bead	35	20	923573

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Capacitors					
C6	6µ8	Tantalum Bead	35	20	923573
C7	6µ8	Tantalum Bead	35	20	923573
C8	1n	Ceramic Disc	500	20	915243
C9	1n	Ceramic Disc	500	20	915243
C10	1n	Ceramic Disc	500	20	915243
C11	1n	Ceramic Disc	500	20	915243
C12	22	Tantalum Bead	16	20	923570
C13	0µ1	Polycarbonate	100	10	931130
C14	0µ1	Polycarbonate	100	10	931130
C15	22	Tantalum Bead	16	20	923570
C16	1µ0	Tantalum Bead	35	20	923571
C17	1µ0	Tantalum Bead	35	20	923571
C18	1µ0	Tantalum Bead	35	20	923571
C19	1µ0	Tantalum Bead	35	20	923571
C20	1µ0	Tantalum Bead	35	20	923571
C21	6µ8	Tantalum Bead	35	20	923573
C22	6µ8	Tantalum Bead	35	20	923573
C23	1µ0	Tantalum Bead	35	20	923571
C24	2µ2	Tantalum Bead	35	20	923572
C25	2µ2	Tantalum Bead	35	20	923572
C26	1µ0	Tantalum Bead	35	20	923571
C27	1µ0	Tantalum Bead	35	20	923571
C28	1µ0	Tantalum Bead	35	20	923571
C29	1µ0	Tantalum Bead	35	20	923571
C30	1µ0	Tantalum Bead	35	20	923571
C31	1µ0	Tantalum Bead	35	20	923571
C32	1µ0	Tantalum Bead	35	20	923571
C33	0µ1	Polycarbonate	100	10	931130
C34	0µ1	Polycarbonate	100	10	931130
C35	1µ0	Tantalum Bead	35	20	923571
C36	1µ0	Tantalum Bead	35	20	923571
C37	0µ1	Polycarbonate	100	10	931130
C38	6µ8	Tantalum Bead	35	20	923573
C39	220	Electrolytic	16	+50 -10	941843
C40	15	Tantalum Bead	20	20	922516
C41	6µ8	Tantalum Bead	35	20	923573
C42	6µ8	Tantalum Bead	35	20	923573
C43	6µ8	Tantalum Bead	35	20	923573
C44	1µ0	Tantalum Bead	35	20	923571
C45	0µ1	Polycarbonate	100	10	931130

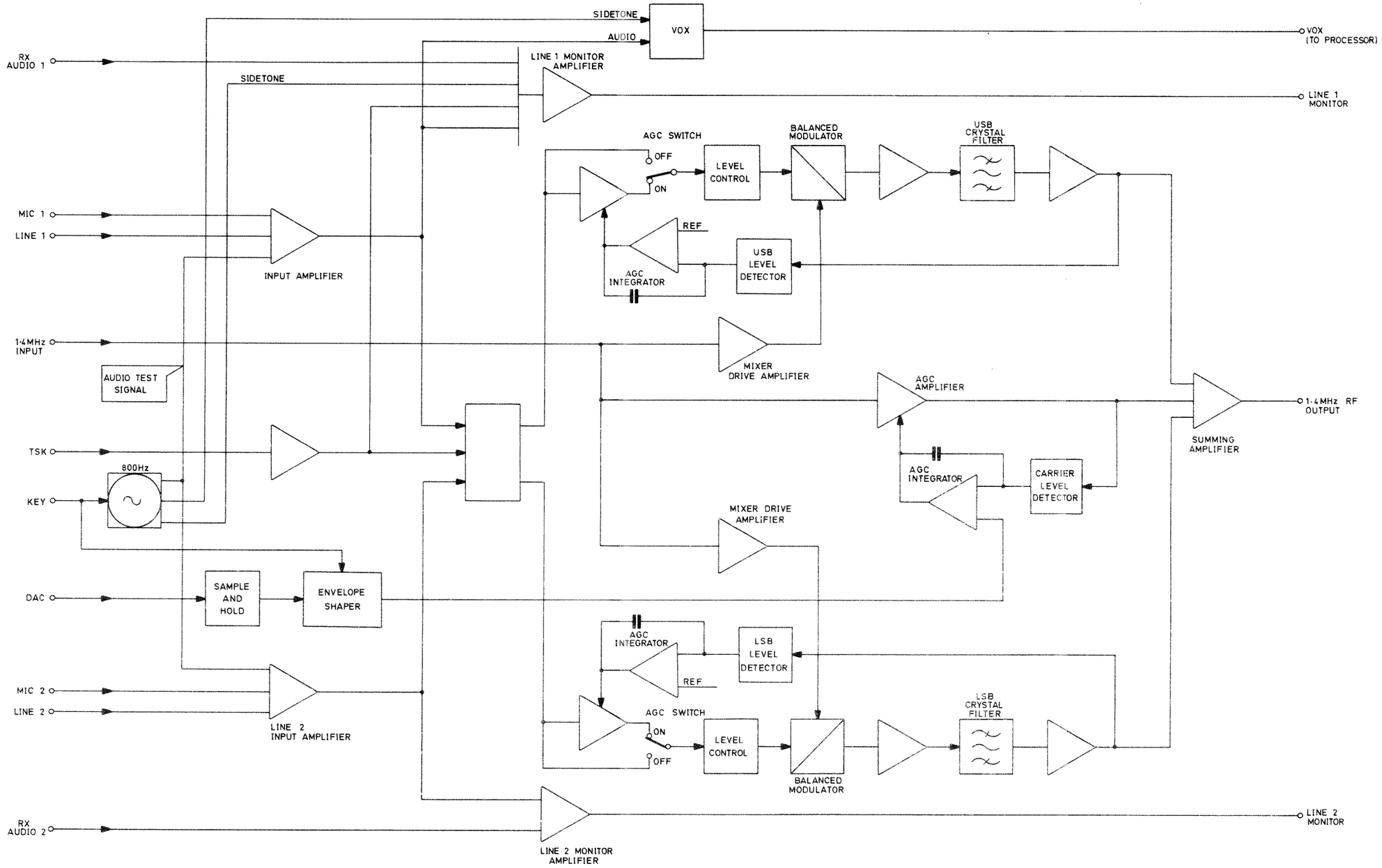
Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Capacitors (cont'd)					
C46	6µ8	Tantalum Bead	35	20	923573
C47	6µ8	Tantalum Bead	35	20	923573
C48	0µ1	Polycarbonate	100	10	931130
C49	10n	Ceramic Disc	250	+40 -20	900067
C50	0µ1	Polycarbonate	100	10	931130
C51	10n	Ceramic Disc	250	+40 -20	900067
C52	0µ1	Polycarbonate	100	10	931130
C53	10n	Ceramic Disc	250	+40 -20	900067
C54	10n	Ceramic Disc	250	+40 -20	900067
C55	10n	Ceramic Disc	250	+40 -20	900067
C56	10n	Ceramic Disc	250	+40 -20	900067
C57	6µ8	Tantalum Bead	35	20	923573
C58	6µ8	Tantalum Bead	35	20	923573
C59	10n	Ceramic Disc	250	+40 -20	900067
C60	0µ1	Polycarbonate	100	10	931130
C61	10n	Ceramic Disc	250	+40 -20	900067
C62	0µ1	Polycarbonate	100	10	931130
C63	10n	Ceramic Disc	250	+40 -20	900067
C64	0µ1	Polycarbonate	100	10	931130
C65	10n	Ceramic Disc	250	+40 -20	900067
C66	10n	Ceramic Disc	250	+40 -20	900067
C67	10n	Ceramic Disc	250	+40 -20	900067
C68	68p	Ceramic Disc	500	10	917737
C69	68p	Ceramic Disc	500	10	917737
C70	68p	Ceramic Disc	500	10	917737
C71	68p	Ceramic Disc	500	10	917737
C72	0µ1	Polycarbonate	100	10	931130
C73	10n	Ceramic Disc	250	+40 -20	900067
C74	10n	Ceramic Disc	250	+40 -20	900067
C75	0µ1	Polycarbonate	100	10	931130
C76	0µ1	Polycarbonate	100	10	931130
C77	0µ1	Polycarbonate	100	10	931130
C78	0µ1	Polycarbonate	100	10	931130
C79	10n	Ceramic Disc	250	+40 -20	900067
C80	10n	Ceramic Disc	250	+40 -20	900067
C81	0µ1	Polycarbonate	100	10	931130
C82	100	Electrolytic	40	+50 -10	940766
C83	47n	Polycarbonate	250	10	935141
C84	0µ1	Polycarbonate	100	10	931130
C85	10n	Ceramic Disc	250	+40 -20	900067

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Capacitors (cont'd)					
C86	10n	Ceramic Disc	250	+40 -20	900067
C87	22n	Polycarbonate	400	10	931137
C88	0µ15	Polycarbonate	100	10	939925
C89	0µ22	Polycarbonate	100	10	931131
C90	10n	Ceramic Disc	250	+40 -20	900067
C91	10n	Ceramic Disc	250	+40 -20	900067
C92	10n	Ceramic Disc	250	+40 -20	900067
C93	0µ22	Polycarbonate	100	10	931131
C94	0µ1	Polycarbonate	100	10	931130
C95	0µ1	Polycarbonate	100	10	931130
C96	10n	Ceramic Disc	250	+40 -20	900067
C97	0µ1	Polycarbonate	100	10	931130
C98	150p	Silver Mica	100	2	931614
C99	10n	Ceramic Disc	250	+40 -20	900067
C100	0µ1	Polycarbonate	100	10	931130
C101	10n	Ceramic Disc	250	+40 -20	900067
C102	10n	Ceramic Disc	250	+40 -20	900067
C103	22n	Polycarbonate	400	10	931137
C104	0µ1	Polycarbonate	100	10	931130
C105	1n	Ceramic Disc	500	20	915243
C106	10n	Ceramic Disc	250	+40-20	900067
Inductors					
L1	10µH	Choke		10	922364
L2	100µH	Choke		10	939161
L3	10µH	Choke		10	922364
Transformers					
T1		Transformer Assembly			AT82403
T2		Transformer Assembly			AT82403
T3		Transformer Assembly			AT82404
T4		Transformer Assembly			AT82404
T5		Transformer Assembly			AT82405

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Connectors					
PL12		Plug, 40-way			939992
PL13		Plug, 10-way			939988
PL14		Plug, coaxial, 50 ohms			935268
PL15		Plug, coaxial, 50 ohms			935268
Diodes					
D1		Silicon 1N4149			923222
D2		Silicon 1N4149			923222
D3		Silicon 1N4149			923222
D4		BZX79 C6V8			921750
D5		Silicon 1N4149			923222
D6		Silicon 1N4149			923222
D7		Silicon 1N4149			923222
D8		Silicon 1N4149			923222
D9		Silicon 1N4149			923222
D10		Silicon 1N4149			923222
D11		Silicon 1N4149			923222
D12		Silicon 1N4149			923222
D13		Schottky 5082-2811			919460
D14		Schottky 5082-2811			919460
D15		Schottky 5082-2811			919460
D16		Zener, 6.8 V, 400 mW	BZX79C6V8		921750
Transistors					
TR1		NPN Silicon BC109			923234
TR2		NPN Silicon BC109			923234
TR3		NPN Silicon 2N2369			906842
TR4		NPN Silicon 2N2369			906842
TR5		NPN Silicon BC109			923234
TR6		NPN Silicon BC109			923234
TR7		PNP Silicon BFX48			915231
TR8		NPN Silicon BC109			923234
TR9		NPN Silicon BC109			923234
TR10		NPN Silicon BC109			923234

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Transistors (cont'd)					
TR11		NPN Silicon BC109			923234
TR12		PNP Silicon BFX48			915231
TR13		PNP Silicon BFX48			915231
TR14		NPN Silicon BC109			923234
TR15		NPN Silicon BC109			923234
TR16		NPN Silicon BC109			923234
TR17		NPN Silicon BC109			923234
Integrated Circuits					
ML1		Transistor Array 3046			938975
ML2		Quad Analogue Switch 4066			930148
ML3		Quad Operational Amplifier 348			939926
ML4		IF Amplifier 757DC			921201
ML5		4-Channel MUX 4052			930147
ML6		Quad Operational Amplifier 348			939926
ML7		Quad Analogue Switch 4066			930148
ML8		IF Amplifier 757DC			921201
ML9		Diode Array 3039			939927
ML10		Diode Array 3039			939927
ML11		Quad Operational Amplfier 348			939926
ML12		Quad Analogue Switch 4066			930148
ML13		Quad Operational Amplifier 348			939926
ML14		Dual Operational Amplifier CA3240E			933580
ML15		Dual Operational Amplifier CA3240E			933580
ML16		Quad Analogue Switch 4066			930148
ML17		Quad Operational Amplifier 324			933619
ML18		Transistor Array 3046			938975
ML19		Quad D-type latch 4042			930861
ML20		Quad D-type latch 4042			930861
ML21		Quad D-type latch 4042			930861
ML22		Quad D-type latch 4042			930861
ML23		Dual Multivibrator 4528			931017
ML24		8-Channel MUX 4051			930035
ML25		Quad Operational Amplifier 324			933619
ML26		Level Shifter 40109			931054
ML27		Level Shifter 40109			931054
ML28		Level Shifter 40109			931054
ML29		Quad D-type latch 4042			930861
ML30		Quad 2-input OR gate 4071			930038

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Integrated Circuits (cont'd)					
ML31		Multivibrator 4047			930992
ML32		Dual 2-input NAND buffer 40107			931052
ML33		+5 V Regulator 78L05AWC			926425
ML34		+12 V Regulator 78M12HC			936256
ML35		-12 V Regulator 79M12AHC			938563
Miscellaneous					
		Test Point			936148
		Captive Fastener			930396
		8-pin DIL IC socket			940901
		14-pin DIL IC socket			940902
		16-pin DIL IC socket			940903
SA,SB		Switch, 2-way SPST			932881



RACAL
TH3071

Simplified Block Diagram
Modulation Board

Fig. 10·1

FROM SHEET 2

a AUDIO TEST TONE IN
b AUDIO SIDETONE IN
c AUDIO SIDETONE IN
d BOARD OUTPUT LEVEL DETECTOR
e USB LEVEL DETECTOR OUTPUT
f LSB LEVEL DETECTOR OUTPUT

MIC 1
LINE 1 SIG.
LINE 1 GND.
TSK
RX AUDIO 1
MIC 2
LINE 2 SIGNAL
LINE 2 GND
RX AUDIO 2

ML5 ML4 ML2a ML2b ML3a ML3b ML3c ML3d ML17a ML17b ML17c ML17d ML16a ML16b ML6a ML6b ML6c ML6d ML7a ML7b ML7c ML7d ML8 ML25a ML25b ML25c ML15a ML19 ML21 ML26 ML28

TP1 TP2 TP3 TP4 TP5 TP6

LINE 2 MONITOR
LINE 1 MONITOR
LINE 2 METER
LINE 1 METER

RACAL

TH3071-DC87649 | 10 2 | 1 | V2

INTEGRATED CIRCUITS						
REF	TYPE	-12V	0V	+5V	+12V	+15V
ML2,7,16	4066	—	7	—	14	—
ML3,6	348	11	—	—	4	—
ML4,8	757DC	—	5	—	11	—
ML5	4052	—	7,8	—	16	—
ML14	3240E	4	—	—	—	8
ML15	3240E	—	4	—	8	—
ML17,25	324	—	11	—	4	—
ML19,20,21	4042	—	8	—	16	—
ML23	4528	—	8	—	16	—
ML24	4051	—	8	—	16	—
ML26,27,28	40109	—	8	1	16	—
ML30,	4071	—	7	—	14	—
ML33	78L05	—	—	—	—	—
ML34	78M12	—	—	—	—	—
ML35	79M12	—	—	—	—	—

TRANSISTORS	
TR1,2	BC109
DIODES	
D1-6, 9	IN4149

Circuit : Modulation Board (Sheet 1)

Fig. 10.2

MIXER DRIVE AMPLIFIER

BALANCED MODULATOR
INPUTS 1·4MHz CARRIER AND AUDIO
OUTPUT 1·4MHz DOUBLE SIDEBAND SUPPRESSED CARRIER

AMPLIFIER

1·4MHz USB FILTER
(GENERATED AS LSB AT THIS POINT DUE TO FREQUENCY INVERSION ON MIXER BOARD)

AMPLIFIER

SUMMING AMPLIFIER

PL15 1·4 MHz INPUT

B USB AUDIO IN FROM SHEET 1

C LSB AUDIO IN FROM SHEET 1

A STROBE 2B FROM SHEET 1

DATA BUS D0 D7 FROM SHEET 1

FROM SHEET 1 D

FROM SHEET 1 E

9·8V USB ON 12V USB OFF

250mV pk-pk

TP10

USB LEVEL DETECTOR

e TO ML17b (SHEET 1)

0·75V FOR 0dBm USB O/P AT PL14

USB LEVEL

500mV pk-pk

9·8V LSB ON 12V LSB OFF

TP12

LSB LEVEL

LOW POWER

LSB LEVEL DETECTOR

f TO ML25a (SHEET 1)

0·75V FOR 0dBm LSB O/P AT PL14

ADJUSTMENTS
SET T5 FOR M
SET R161 FOR
OF 0dBm AT PL
WITH USB AC
0dBm AT PL14
WITH LSB AC
0dBm AT PL14

TP14

CARRIER LEVEL

GAIN CONTROLLED 1·4MHz CARRIER AMPLIFIER

CARRIER LEVEL DETECTOR

COMPARATOR

AGC INTEGRATOR

8·2V FOR DSB CARRIER

8·2V FOR 0dB CARRIER

B5 FROM ML39

SAMPLE AND HOLD

CARRIER ON/OFF SWITCH

KEYS ENVELOPE SHAPER

RANGE SELECTOR

CARRIER ON/OFF LOGIC

1=DAC SAMPLE

1=CARRIER ON

B7 TO ML16c

B5 TO ML12c

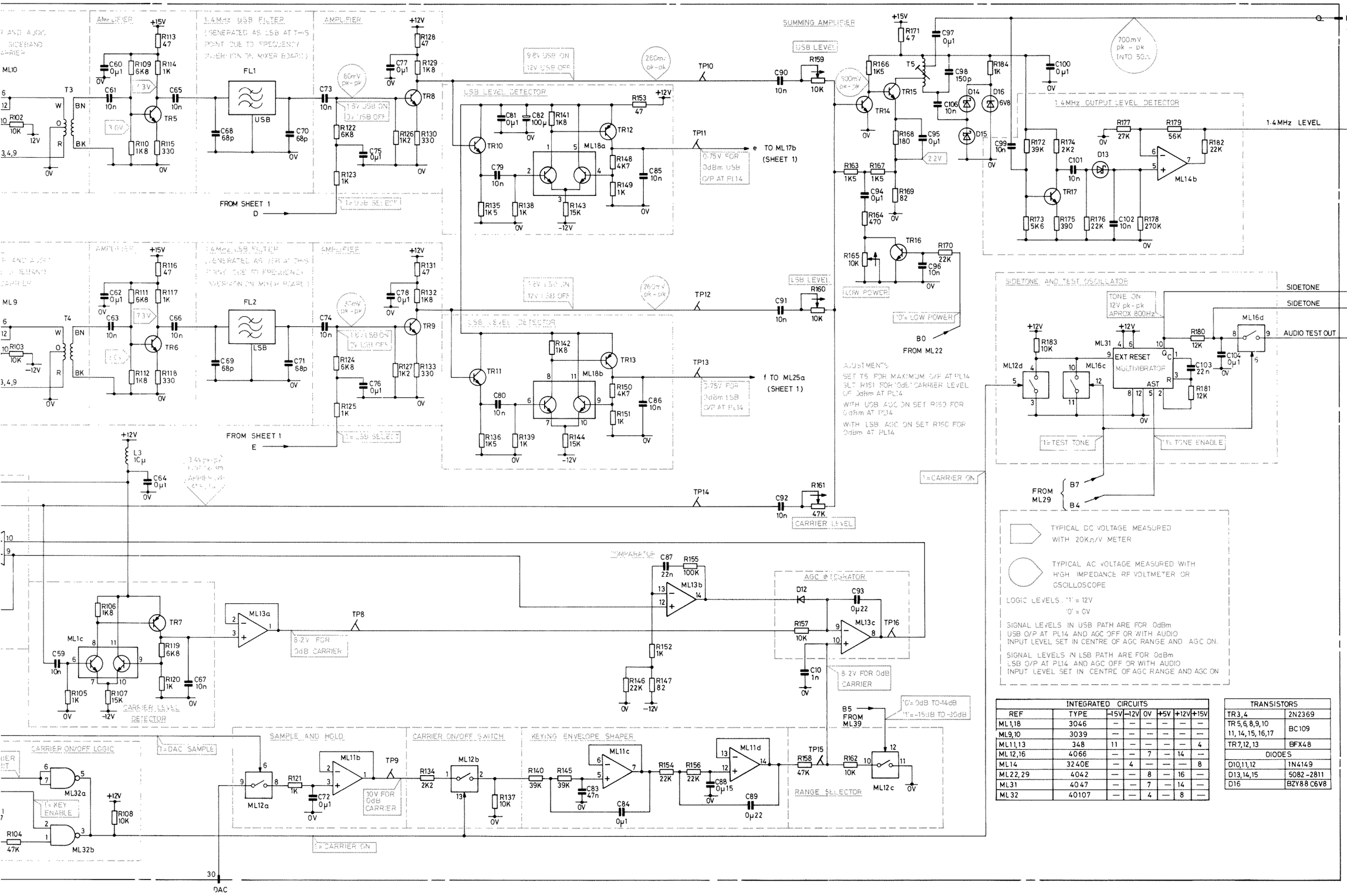
B4 TO ML31

B0 TO R170

KEY DOWN

PL12 25 KEY

30 DAC



TYPICAL DC VOLTAGE MEASURED WITH 20KΩ/V METER

TYPICAL AC VOLTAGE MEASURED WITH HIGH IMPEDANCE RF VOLTMETER OR OSCILLOSCOPE

LOGIC LEVELS. '1' = 12V
'0' = 0V

SIGNAL LEVELS IN USB PATH ARE FOR 0dBm USB O/P AT PL14 AND AGC OFF OR WITH AUDIO INPUT LEVEL SET IN CENTRE OF AGC RANGE AND AGC ON.

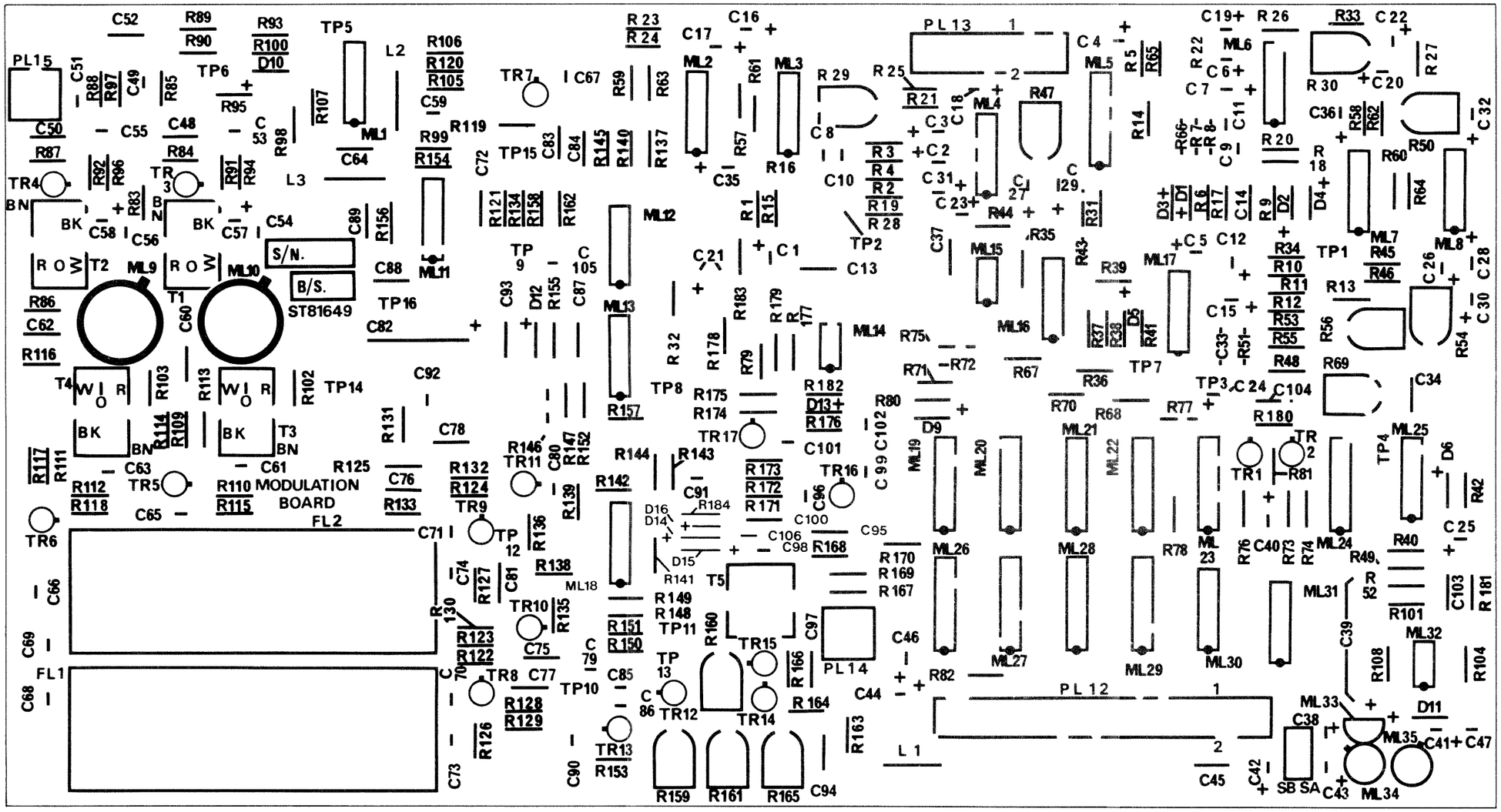
SIGNAL LEVELS IN LSB PATH ARE FOR 0dBm LSB O/P AT PL14 AND AGC OFF OR WITH AUDIO INPUT LEVEL SET IN CENTRE OF AGC RANGE AND AGC ON

INTEGRATED CIRCUITS							
REF	TYPE	-15V	-12V	0V	+5V	+12V	+15V
ML1,18	3046	—	—	—	—	—	—
ML9,10	3039	—	—	—	—	—	—
ML11,13	348	11	—	—	—	—	4
ML12,16	4066	—	—	7	—	14	—
ML14	3240E	—	—	4	—	—	8
ML22,29	4042	—	—	8	—	16	—
ML31	4047	—	—	7	—	14	—
ML32	40107	—	—	4	—	8	—

TRANSISTORS	
TR3,4	2N2369
TR5,6,8,9,10 11,14,15,16,17	BC109
TR7,12,13	BFX48
DIODES	
D10,11,12	1N4149
D13,14,15	5082-2811
D16	BZY88 C6V8

Circuit: Modulation Board (Sheet 2)

Fig.10.3



RACAL

TH 3071	EA81648/4
2	

Layout: Modulation Board Fig 10.4

CHAPTER 11

RF OUTPUT BOARD

CONTENTS

Illustrations

CHAPTER 11

RF OUTPUT BOARD

INTRODUCTION

1. This board accepts the 1 MHz to 30 MHz output signal from the mixer board (Chapter 9) and provides the final RF output signal at a preset level between 25 mW and 200 mW.

CIRCUIT DESCRIPTION (Fig. 11.1)

2. The input signal from the mixer board, at coaxial connector PL22, is applied to the emitter of TR1 via the preset level control resistor R1 and transformer T1. Transistors TR1, TR2 and TR3 are connected as a broad-band, transformer - coupled (interstage transformers T2 and T3), RF amplifier. The +20 V supply for the amplifier transistors is controlled by switching transistor TR4, which in turn is controlled by the level at the $\overline{\text{MUTE}}$ input, PL21 pin 4 (from the front panel interface board). When the mute condition is not preset, the voltage at TP4 rises to approximately +10 V, TR5 is turned on, and this in turn causes conduction of TR4. When a 0V mute signal is applied, TR5 is turned off, the voltage at the base of TR4 rises to approximately +20 V, and the supply to the amplifier transistors is switched off.

3. Output transformer T4 couples the amplified RF signal at 50 ohms impedance to the BNC RF output socket on the rear panel, and via R20 to the RF monitor socket on the front panel.

4. The RF output level detector D1, ML1, D2, produces a d.c. output voltage, the level of which is proportional to the peak envelope voltage. This d.c. output voltage is applied to the front panel interface board where it is used for metering purposes.

RF OUTPUT BOARD (ST81653)

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Resistors			**Watts**		
R1	220	Variable, Preset	0.5	20	924869
R2	2k2	Metal Oxide	0.25	2	916546
R3	470	Metal Oxide	0.25	2	920758
R4	56	Metal Oxide	0.25	2	917055
R5	56	Metal Oxide	0.25	2	917055
R6	1k5	Metal Oxide	0.25	2	911166
R7	680	Metal Oxide	0.25	2	910113
R8	56	Metal Oxide	0.25	2	917055
R9	390	Metal Oxide	0.25	2	916331
R10	82	Metal Oxide	0.25	2	909550
R11	1k	Metal Oxide	0.25	2	913489
R12	470	Metal Oxide	0.25	2	920758
R13	56	Metal Oxide	0.25	2	917055
R14	68	Metal Oxide	0.25	2	930480
R15	68k	Metal Oxide	0.25	2	916478
R16	2k2	Metal Oxide	0.25	2	916546
R17	270k	Metal Oxide	0.25	2	923598
R18	56k	Metal Oxide	0.25	2	913497
R19	22k	Metal Oxide	0.25	2	913493
R20	1k	Metal Oxide	0.25	2	913489
R21	100	Metal Oxide	0.25	2	910388
R22	10k	Metal Oxide	0.25	2	914042
R23	10k	Metal Oxide	0.25	2	914042
R24	1k	Metal Oxide	0.25	2	913489
Capacitors			**Volts**		
C1	4µ7	Tantalum Bead	50	20	939893
C2	0µ1	Ceramic Plate	100	20	939892
C3	0µ1	Ceramic Plate	100	20	939892
C4	0µ1	Ceramic Plate	100	20	939892
C5	4µ7	Tantalum Bead	50	20	939893
C6	0µ1	Ceramic Plate	100	20	939892
C7	0µ1	Ceramic Plate	100	20	939892
C8	0µ1	Ceramic Plate	100	20	939892
C9	4µ7	Tantalum Bead	50	20	939893
C10	0µ1	Ceramic Plate	100	20	939892

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Capacitors (cont'd)					
C11	0µ1	Ceramic Plate	100	20	939892
C12	0µ1	Ceramic Plate	100	20	939892
C13	0µ1	Ceramic Plate	100	20	939892
C14	100p	Ceramic Disc	500	20	917417
C15	4µ7	Tantalum Bead	50	20	939893
C16	0µ1	Ceramic Plate	100	20	939892
C17	1µ0	Tantalum Bead	35	20	923571
Inductors					
L1	3µ3H	Choke		10	940025
Transformers					
T1		Transformer Assembly			AT82408
T2		Transformer Assembly			AT82386
T3		Transformer Assembly			AT82386
T4		Transformer Assembly			AT82386
Connectors					
PL21		Plug, 10-way			937704
PL22		Plug, coaxial, 50 ohms			935268
PL23		Plug, coaxial, 50 ohms			935268
PL24		Plug, coaxial, 50 ohms			935268
Diodes					
D1		Schottky 5082-2811			919460
D2		Silicon 1N4149			923222

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Transistors					
TR1		NPN Silicon BFW17A			920012
TR2		NPN Silicon BFW17A			920012
TR3		NPN Silicon BFW17A			920012
TR4		PNP Silicon 2N4037			922991
TR5		NPN Silicon BC109			923234
Integrated Circuits					
ML1		Operational Amplfiier CA3140E			932204
Miscellaneous					
TP1-TP5		Test Point			936148
FX1-FX6		Ferrite Bead FX1115			900461
		Captive Fastener			930396
		8-pin DIL IC socket			930604
		Heatsink (for TR1, TR2, TR3)			905416

VOLTAGE MEASUREMENTS MADE WITH OUTPUT FREQUENCY 2MHz AND LEVEL 200mW

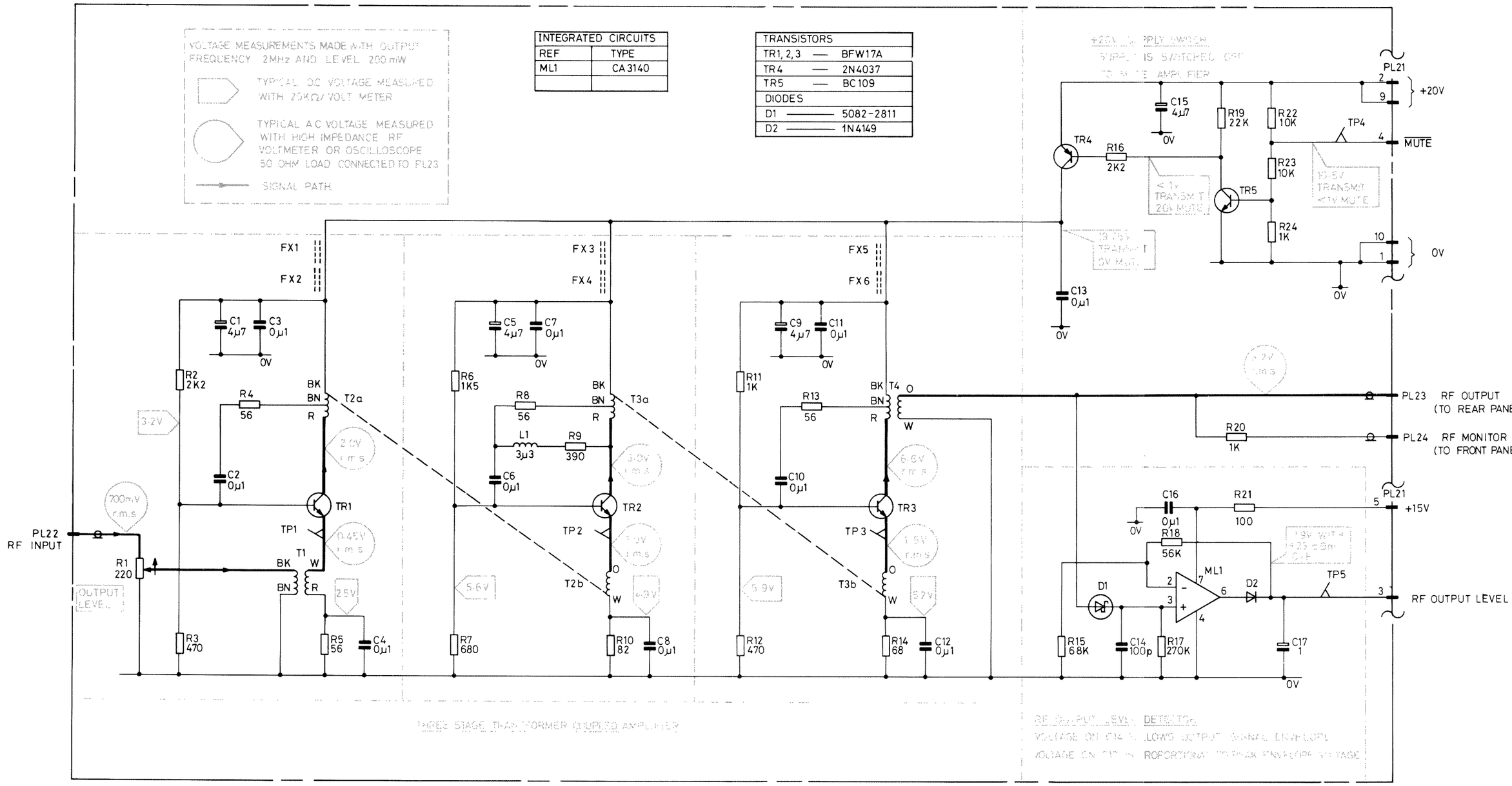
TYPICAL DC VOLTAGE MEASURED WITH 20KΩ/VOLT METER

TYPICAL A.C VOLTAGE MEASURED WITH HIGH IMPEDANCE RF VOLTMETER OR OSCILLOSCOPE 50 OHM LOAD CONNECTED TO PL23

SIGNAL PATH

INTEGRATED CIRCUITS	
REF	TYPE
ML1	CA3140

TRANSISTORS	
TR1, 2, 3	BFW17A
TR4	2N4037
TR5	BC109
DIODES	
D1	5082-2811
D2	1N4149



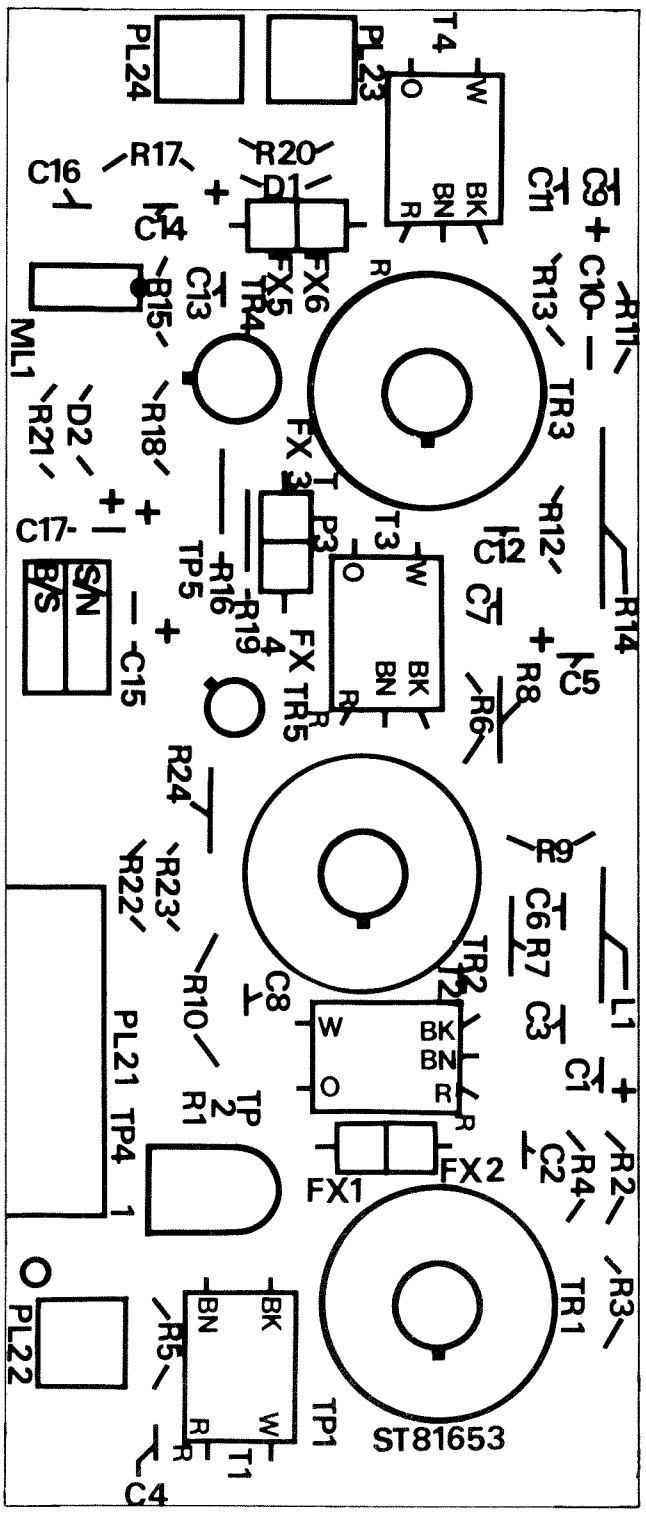
RACAL

TH3071	DC81653	11·1
2		1/2

TH3071 DC81653 11·1 2 2/2

Circuit : RF Output Board

Fig.11·1



RACAL

TH 3071	CA 81652/4
2	

Layout : RF Output Board

Fig.11.2

CHAPTER 12

REAR PANEL BOARD

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CHAPTER 12

REAR PANEL BOARD

INTRODUCTION

1. The rear panel board, as the name implies, is mounted on the inner face of the rear panel. It houses the multi-way rear-panel sockets (SK4, SK5, SK6) with associated de-coupling components, and the audio line 1 and line 2 600 ohm isolation transformers (T1, T2).

CIRCUIT DESCRIPTION

2. The circuit diagram of the rear panel board is given in fig. 12.1, and is self-explanatory.

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number

REAR PANEL BOARD (ST81655)

Resistors

R1	560	Metal Oxide		2	917061
R2	560	Metal Oxide		2	917061
R3		Not Fitted			
R4		Not Fitted			

Capacitors

			Volts		
C1-C26	10n	Ceramic Disc	250	+40 -20	900067
C27		Not Fitted			
C28-C32	10n	Ceramic Disc	250	+40 -20	900067
C33		Not Fitted			
C34-C36	10n	Ceramic Disc	250	+40 -20	900067
C37		Not Fitted			
C38-C40	10n	Ceramic Disc	250	+40 -20	900067
C41		Not Fitted			
C42-C44	10n	Ceramic Disc	250	+40 -20	900067
C45-C53		Not Fitted			

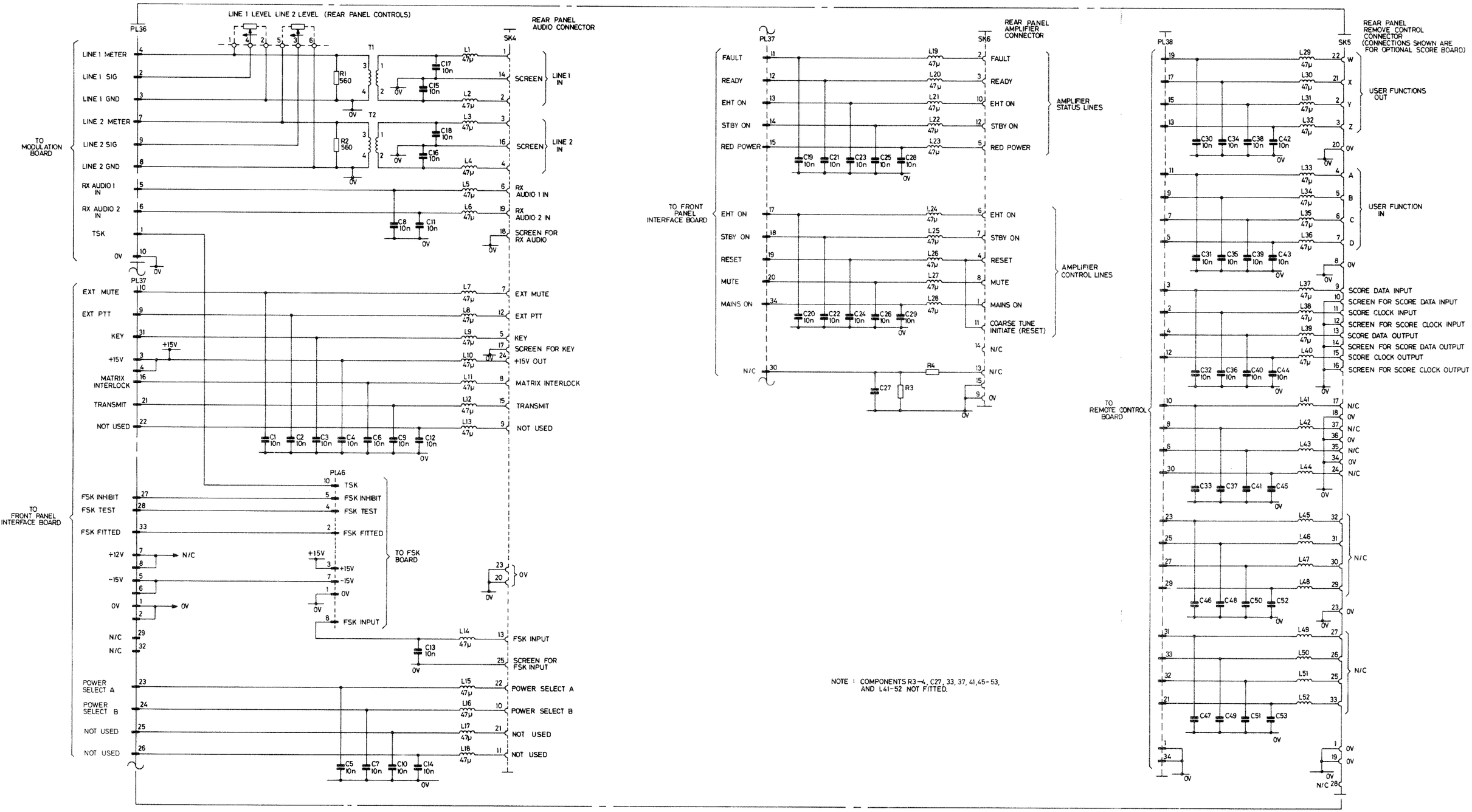
Inductors

L1-L40	47µH	Choke	10	939160
L41-L52		Not Fitted		

Transformers

T1	Transformer Assembly	AT82412
T2	Transformer Assembly	AT82412

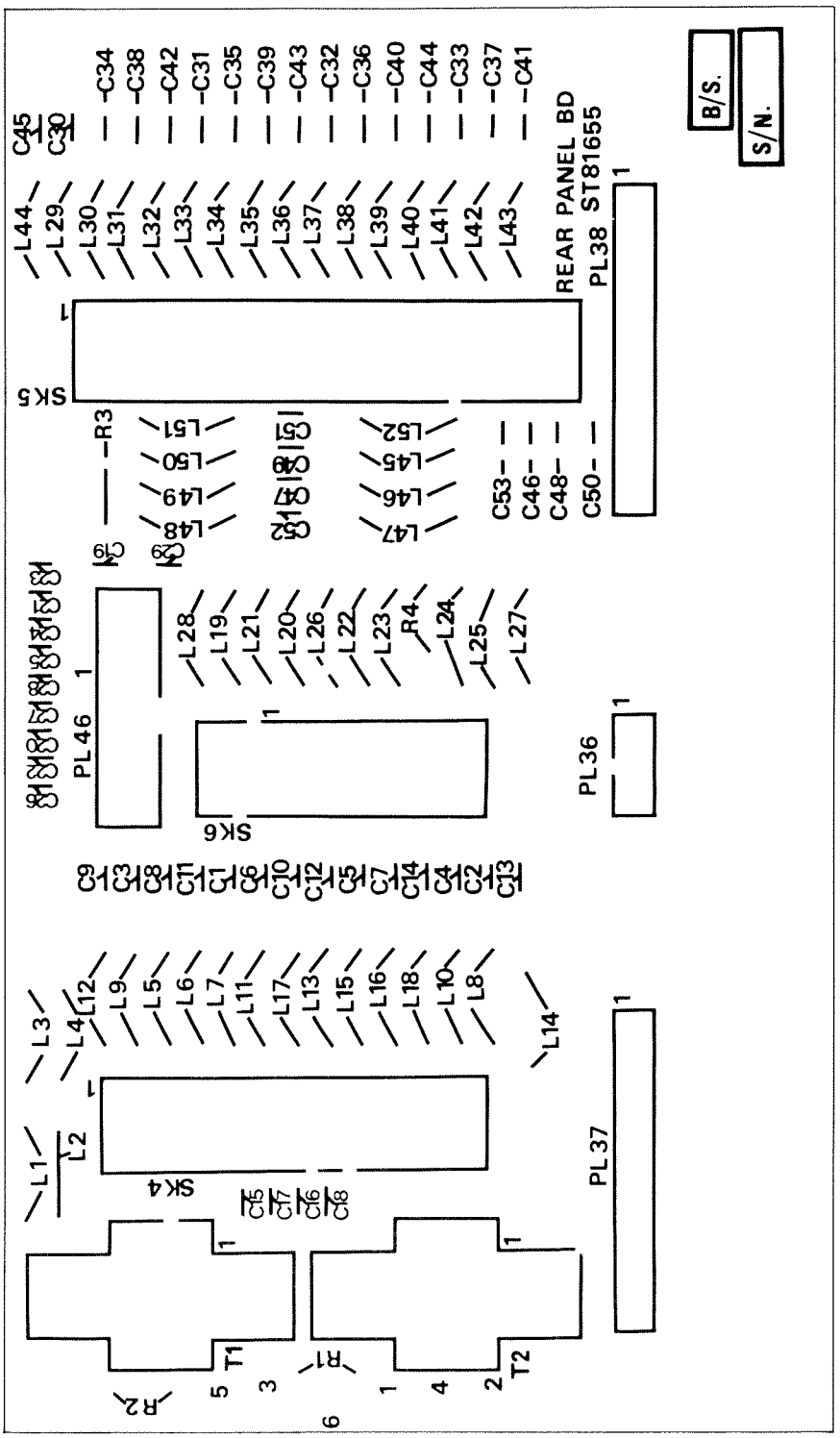
Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Connectors					
PL36		Plug, 10-way			939979
PL37		Plug, 34-way			939983
PL38		Plug, 34-way			939983
PL46		Plug, 10-way			939988
SK4		Socket, 25-way			930819
SK5		Socket, 37-way			930820
SK6		Socket, 15-way			939891
Miscellaneous					
		Captive Fastener			930396



RACAL

TH 3071	DC81655
2	

Circuit : Rear Panel Board Fig.12.1



RACAL

TH 3071	DA 81654/4
1	

Layout: Rear Panel Board

Fig.12.2

CHAPTER 13

POWER SUPPLY MODULE

CONTENTS

Illustrations

CHAPTER 13

POWER SUPPLY MODULE

INTRODUCTION

1. The power supply module provides regulated outputs at +20 V, +15 V, +12 V, +5 V, -15 V and -30 V, and two 10 V unregulated outputs (designated +5 V UNREG A and B). It is a self-contained module and can be removed from the unit as a complete assembly.

CIRCUIT DESCRIPTION (Fig. 13.1)

2. The power input connector PL1, fuse FS1, supply filter components and the voltage selector are all combined in one unit. The voltage selector consists of a small printed circuit card which can be inserted in one of four different ways to suit an input voltage of 100 V, 120 V, 220 V or 240 V nominal. Bridge rectifier D1 feeds the +20 V regulator ML2, D2 feeds the +15 V regulator ML3, D3 feeds the +5 V regulator ML5, and D4 feeds the -30 V regulator ML6. The +12 V supply is derived from the +15 V supply (by ML4), and similarly, the -15 V supply is derived from the -30 V supply (by ML1).

3. The +20 V regulator device ML2 is of the adjustable output type, where resistors R1 and R2 are used to select the required output voltage.

   The -30 V regulator ML6 is of similar construction and includes a preset resistor R5 to accurately set the output level. The remaining regulators are all of the fixed-voltage, three-terminal type. ML2, ML3, ML4 and ML5 are all mounted on the module rear face, ML6 is mounted on the module front face, and ML1 is mounted on the small internal board. All six regulator devices each contain a current limiting circuit to limit the peak current to a safe value. If the internal power dissipation becomes too high for the heat sinking provided, a thermal shut-down circuit takes over to prevent the device overheating.

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number

POWER SUPPLY MODULE (ST80548)

Resistors

*R1	220	Metal Oxide	2	910390
*R2	3k3	Metal Oxide	2	910111
*R3	220	Metal Oxide	2	910390
*R4	4k7	Metal Oxide	2	913490
*R5	1k	Variable, Preset	10	939911
R6		Transient Suppressor		927404

Capacitors

			Volts		
*C1	1µ0	Tantalum Bead	63	20	938981
*C2	1µ0	Tantalum Bead	40	10	931177
C3	2200	Electrolytic	63	+30 -10	940060
C4	2200	Electrolytic	63	+30 -10	940060
C5	1000	Electrolytic	25	+30 -10	939915
C6	0µ1	Tantalum Bead	500	+80 -20	918088
C7	0µ1	Tantalum Bead	500	+80 -20	918088
C8	1µ0	Tantalum Bead	50	20	939931
C9	1µ0	Tantalum Bead	40	20	931177
C10	470	Electrolytic	100	+30 -10	939913
C11	1µ0	Tantalum Bead	40	20	931177
C12	0µ1	Tantalum Bead	500	+80 -20	918088
C13	0µ1	Tantalum Bead	500	+80 -20	918088
C14	1µ0	Tantalum Bead	40	20	931177
C15	1µ0	Tantalum Bead	40	20	931177
C16	1µ0	Tantalum Bead	63	20	938981

* Mounted on power supply board ST81661

Transformers

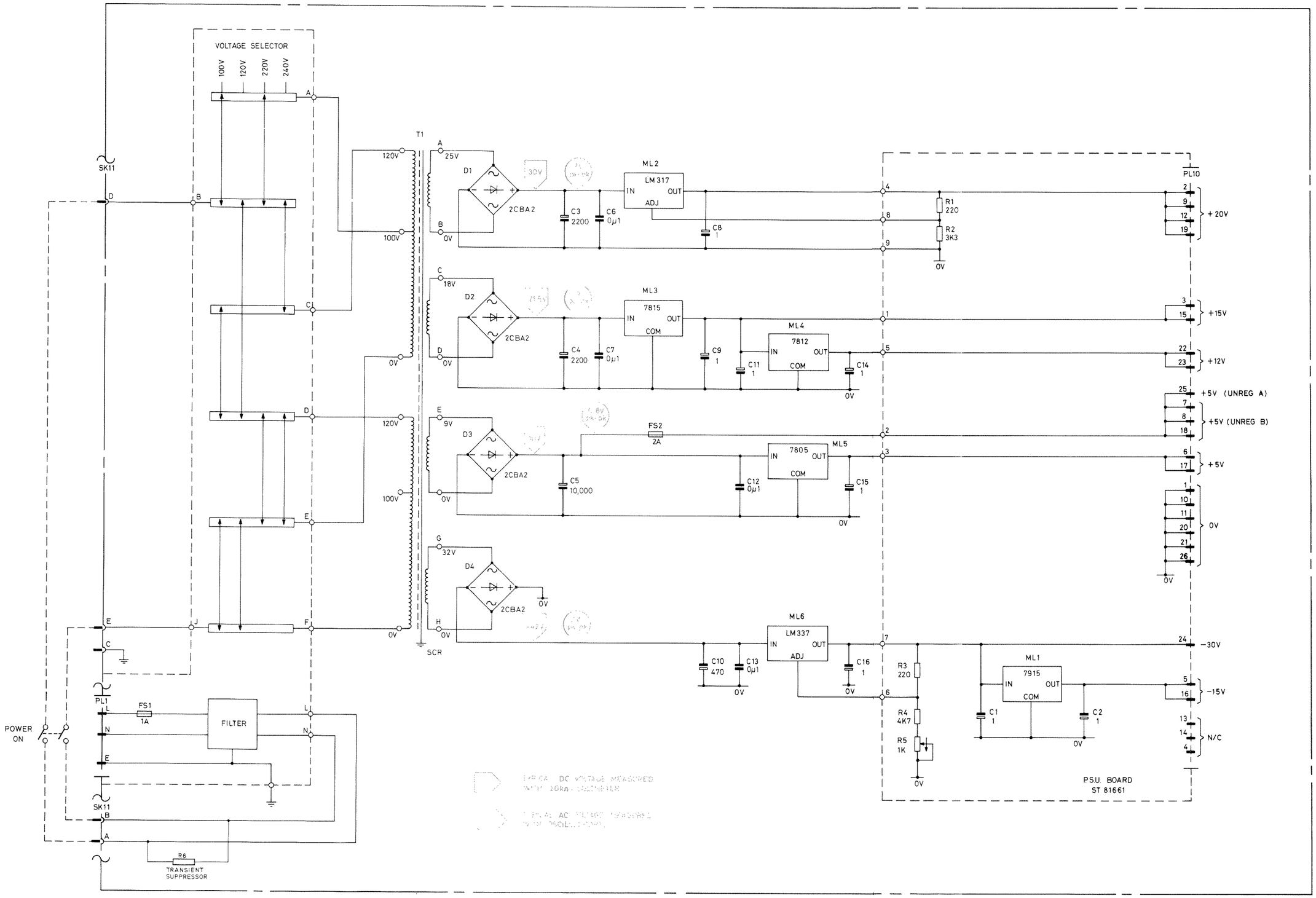
T1	Power Transformer	CT82431

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Connectors					
PL1		3-way power input module			937173
*PL10		Plug, 26-way			939990
SK11		Socket, 5-way			928267
Fuses					
FS1	1A, 250 V	Fuse link, time lag			934804
FS2	2A	Fuse link			922449
		Fuseholder (FS2)			930381
Diodes					
D1		Bridge Rectifier, SCBA2			929915
D2		Bridge Rectifier, SCBA2			929915
D3		Bridge Rectifier, SCBA2			929915
D4		Bridge Rectifier, SCBA2			929915
Integrated Circuits					
*ML1		-15 V Regulator 7915			939916
ML2		Adjustable Positive Regulator LM317k			932798
ML3		+15 V Regulator 7815KC			932797
ML4		+12 V Regulator 7812KC			923014
ML5		+5 V Regulator 7805KC			922259
ML6		Adjustable Negative Regulator LM337HVK			939930

* Mounted on power supply board ST81661

Miscellaneous

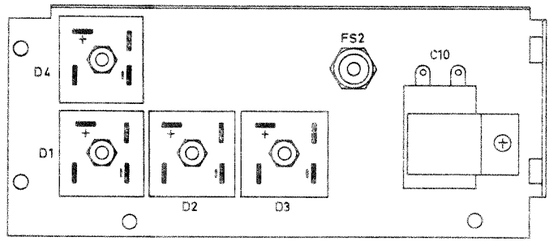
Power Supply Board	ST81661
Captive Screw	AD80541
Heatsink	BD80540
Transistor Cover	932772

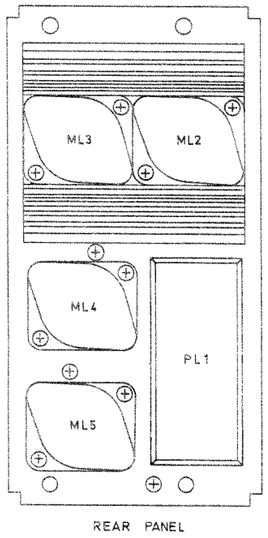


RACAL

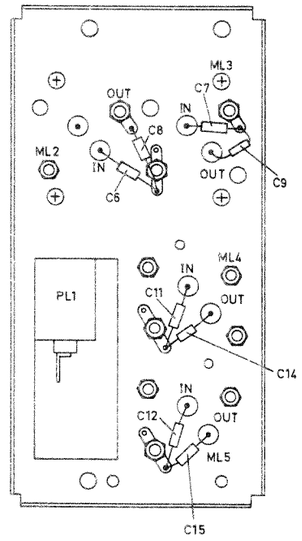
TH3071	DC80548	13-1	TH3071	DC80548	13-1
2		1/2	2		2/2

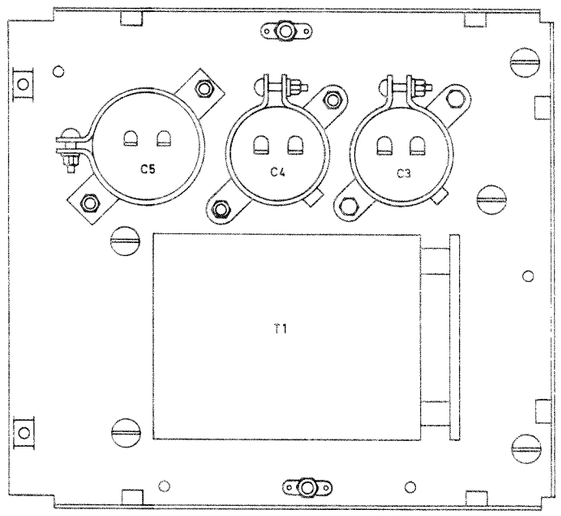
Circuit : Power Supply Module **Fig.13-1**

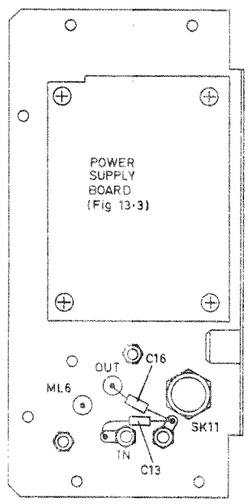


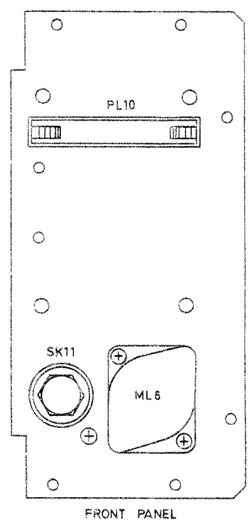


REAR PANEL

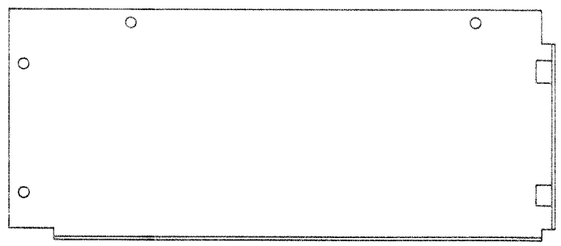






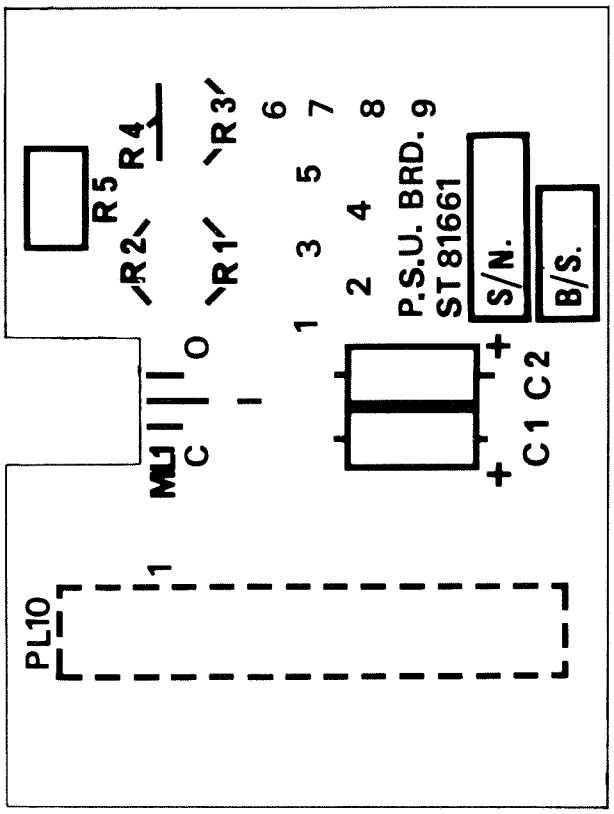


FRONT PANEL



RACAL
TH3071

Layout : Power Supply Module Fig.13·2



RACAL

TH 3071	CA 81660/4
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Layout: Power Supply Board

Fig.13.3

CHAPTER 14

SCORE INTERFACE BOARD

CONTENTS

CHAPTER 14

SCORE INTERFACE BOARD

INTRODUCTION

1. The SCORE (Serial Control of Racal Equipment) interface board is an optional internally fitted board which provides for extended or remote control of the drive unit, using a control unit such as the Racal MA 1090. The SCORE control system is described in the following paragraphs.

SCORE FORMAT

2. The SCORE format for serial control is designed to cater for numerous applications and contains ample additional capacity for expansion. It is based on a number of 48-bit synchronous frames, each of which contain a 16-bit preamble (synchronisation, word number identification, etc.) followed by a 32-bit data word. The total capacity of the system is sixteen 32-bit data words which is equivalent to approximately 400 separate lines. All sixteen words may be revertively checked.

3. Separate lines are used for both data and clock signals travelling in each direction. These comply with CCITT V10 and, over short distances, are compatible with RS232/CCITT V28.

4. The SCORE format for the words used by the MA 1723 (word numbers 0, 1 and 3) is given in Table 1. Although word 0 may be sent as part of a control data sequence, it does not contain any control information and is used only for revertive data.

ROUTINE AND NEW DATA

5. Under static conditions, i.e. when the forward control data does not contain change-of-function information, 'routine data' frames are sent in numerical sequence, and at a rate determined by the SCORE clock frequency. When a change-of-function is made however, instead of allowing the transfer of the full sequence of frames to occur before the change-of-function is executed at the drive unit, the next frame to be sent will contain the data word carrying the change-of-function information. Thus the frames are sent out of numerical sequence and priority is given to those frames containing new data. This is achieved under software control where a flag is set each time a control setting is changed to indicate that the appropriate word requires transmission. The flag is reset when the data word is transmitted.

FRAME COMPARISON

6. Error detection is accomplished by the use of the frame comparison technique, which means that two identical frames must be received at the drive unit before a change-of-function can occur.

TABLE 1: SCORE DATA FORMAT

	BIT No.	BIT FUNCTION OR FORCED STATE	MONITOR (0)	FREQUENCY (1)	TRANSMIT MODE (3)	
PREAMBLE						
	0	0				
	1	1				
	2	1 SYNC				
	3	1 CODE				
	4	1				
	5	1				
	6	TRANSMIT				
	7	RECEIVE				
	8	CONTROL INHIBIT RETURN MONITOR				
	10	ADDRESS	0	0	0	
	11	EQUIPMENT	0	0	0	
	12	1 DATA	0	1	1	
	13	2 WORD	0	0	1	
	14	4 IDENT	0	0	0	
	15	8	0	0	0	
DATA WORD						
	16		A	0	STANDBY	16
	17		B USER	0 NOT	EHT ON	17
	18		C FUNCTION	0 USED	RESET	18
	19		D	0	0	19
	20		0	0	0	20
	21		0 NOT	0	0 NOT	21
	22		0 USED	0	0 USED	22
	23		0	0	0	23
	24		STANDBY	1	0	24
	25		0	2	-6 CARRIER	25
	26		EHT ON	4 100 Hz	-10 LEVEL	26
	27		CONTROL ON	8	-20	27
	28		READY	1	1	28
	29		0	2	2 MODE	29
	30		0	4 kHz	4	30
	31		REDUCED POWER	8	8	31
	32		TRANSMIT	1	SYMMETRICAL	32
	33		FAULT	2	1 DRIVE UNIT	33
	34		FC ERROR	4 10 kHz	2 STATE	34
	35		0	8	0	35
	36		0	1	HIGH PWR.	36
	37		0	2	AUTO RESET	37
	38		0	4 100 kHz	VOX	38
	39		0	8	0	39
	40		0 NOT USED	1	0 LOW	40
	41		0	2	A | POWER	41
	42		0	4 MHz	B | SELECT	42
	43		0	8	0	43
	44		0	1 10 MHz	W	44
	45		0	2	X USER	45
	46		0	0 NOT	Y FUNCTION	46
	47		0	0 USED	Z	47

PREAMBLE

7. A 16-bit preamble is added to each 32-bit data word to form one complete 48-bit frame. The preamble contains a 6-bit sync. code, a 2-bit transmit/receive (PTT) code, a control inhibit bit, a return monitor bit, a 2-bit address word security code, and a 4-bit data word identification code; these are described in the following paragraphs.

Sync. Code

8. The sync. code (bits 0 to 5) consists of a '0' followed by five consecutive '1's. The maximum number of consecutive '1's that occur in serial BCD data is four, e.g. BCD seven followed by BCD eight. This then makes five '1's a unique code. For added security, the next two bits of the preamble (used for PTT) may not consist of consecutive '1's. This is done to 'terminate' the sync. code and to prevent the generation of a false sync. code following a line break etc.

Transmit/Receive

9. Bits 6 and 7 of the preamble are used for transmit/receive switching (PTT) where the transmit state may mute a receiver and set the associated transmitter to the transmit condition. As mentioned in para. 8, these two bits must not consist of consecutive '1's. The coding of these bits is as follows:

Bit 7	Bit 6	Function
0	1	TRANSMIT
1	0	RECEIVE
1	1	NOT ALLOWED (fault)

Control Inhibit Bit

10. This bit of the preamble (bit 8) is used, as the name implies, to inhibit the control functions of the drive unit. When it is set to a '1', the drive unit control settings remain unchanged and further control instructions conveyed by the 32-bit data words are ignored. The revertive data however, is returned to the control unit in the normal way. The control inhibit bit is set to a '1', for example, when the drive unit is being controlled by the Racal MA 1090, and CHECK is selected at the MA 1090 front panel.

Return Monitor Bit

11. The return monitor bit is normally at '0' and is set to a '1' in control data frames sent to the drive unit to cause continuous word 0 monitor frames to be returned via the revertive data. Note however, that this bit cannot be set by the MA 1090 transmitter control unit.

Address Security Code

12. Bits 10 and 11 of the preamble are used in words 8 and 9 of the SCORE control system (equipment and operator addressing words respectively) to provide added security against incorrect addressing. These two bits however, are not decoded by the MA 1723.

Data Word Ident

13. The last four bits of the preamble (bits 12 to 15) are used for the data word identification code, in binary format, i.e. 0 to 15 (decimal) or 0 to F (hexadecimal).

DATA WORDS

14. As stated in para. 4, words 0, 1 and 3 are used by the MA 1723. These are described in the following paragraphs which should be read in conjunction with Table 1. Certain words include a number of 'forced zeros' to prevent the possible occurrence of five consecutive '1's which would otherwise be mistaken for the sync. code.

WORD 0 - MONITOR

15. This word is used for revertive signalling only; although it is transferred as part of the forward control sequence, it does not contain any control data.

User Functions

16. The first four bits of revertive data word 0 provide for the revertive user function where up to four earth (0 V) signals applied to the drive unit are reproduced at the control unit (via the serial revertive data). The four bits are labelled A, B, C and D, and correspond with the A, B, C and D input and output connections at the drive unit and control unit respectively.

Revertive Indicators

17. The remaining operative bits of the word 0 data are all concerned with revertive indicators located at the control unit. Bit 24 is set to a '1' at the drive unit to illuminate the STANDBY ON indicator; similarly, bit 26, 27, 28 or 31 is set to a '1' to illuminate the EHT ON, CONTROL ON (REMOTE selected at the MA 1723), READY or REDUCED POWER indicators. Data bit 32 is set to a '1' whenever the MA 1723 is passing traffic (or tuning), whilst bit 33 is set to a '1' to denote a fault condition at the drive unit or associated linear amplifier. Finally, bit 34 is set to a '1' at the drive unit following the detection of three consecutive frame comparison failures.

WORD 1 - FREQUENCY

18. This word is used to convey the frequency setting information to the drive unit, in BCD format, via data bits 24 to 45. The remaining bits are not used.

19. In order to change the operating frequency, two new frequency frames must be received. These are bit-compared and provided they are the same, the new frequency data is stored in a software buffer. The synthesizer will not however, be updated with the new frequency data until word 3 bit 18 (RESET) is set to a '1' and/or word 3 bit 37 (AUTO-RESET) is set to a '1'. If a new frequency frame pair is received and the auto-reset bit (bit 37) is not set to a '1', then the MA 1723 is set to the mute condition and a fault is indicated via word 0 bit 33.

20. When, following a frequency change, the tuning cycle is completed and the transmitter is ready to resume traffic, a revertive READY signal is applied to the control unit via word 0 bit 28.

WORD 3 - TRANSMIT MODE

21. Word 3 contains the STANDBY, EHT and RESET selection, carrier level and MODE switching, drive unit state, high/low power selection, automatic reset and the forward user functions. Data bits 19 to 24, 35 and 39 to 43 are not used.

OFF, STANDBY and EHT ON Selection

22. Data bits 16 and 17 control STANDBY and EHT switching, as follows. Note that the MA 1723 will not accept an EHT ON command if STANDBY has not previously been selected.

Bit 17	Bit 16	Function
0	0	OFF
0	1	STANDBY
1	0	EHT ON
1	1	STANDBY & EHT ON

Manual RESET

23. This bit is used to control the MA 1723 reset function. To reset the synthesizer (and retune a linear amplifier such as the TTA 1885) this bit must be set to a '1' for at least two frames to allow for a successful frame comparison. This is a manual reset facility; automatic reset is provided by bit 37 (see para. 33).

Carrier Level

24. The carrier level is determined by the coding of bits 25, 26 and 27, as tabulated below. If a sideband mode with non-suppressed carrier is selected, the carrier level must lie between -10 dB and -26 dB. Any value outside this range is automatically converted to the nearest value within the range. For compatible AM (A3A), a -6 dB carrier level is selected. When both -6 dB and USB are selected, the AM mode is assumed.

BIT			CARRIER LEVEL
27	26	25	
0	0	0	SUPP CARRIER
0	0	1	-6 dB
0	1	0	-10 dB
0	1	1	-16 dB
1	0	0	-20 dB
1	0	1	-26 dB
1	1	1	NOT ALLOWED

MODE Selection

25. The mode selection data is conveyed to the drive unit via data bits 28 to 32, as tabulated below. Data bit 32 is known as the symmetrical bit, and is only set to a '1' for symmetrical modes i.e. both sidebands present. Note that for historical reasons, provision is included for a non-symmetrical CW mode selection specifically for the MA 1090 transmitter control unit.

MODE	BIT				
	32	31	30	29	28
USB	0	0	0	0	0
LSB	0	0	0	0	1
AM	0	0	0	0	0
CW	1	0	0	1	0
CW (MA 1090)	0	1	0	0	1
FSK	1	0	0	1	1
ISB(USB,LSB)	0	0	0	1	0
ISB(FSK,LSB)	0	0	1	1	0
ISB(FSK,USB)	0	0	1	1	1

Drive Unit State

26. Data bits 33 and 34 determine the drive unit state, as follows:

BIT 34	BIT 33	STATE
0	0	OPERATE
0	1	MUTE
1	0	BROADCAST
1	1	TUNE

Operate

27. When OPERATE is selected, the transmit/receive state is determined by:

(1) the coding of the transmit/receive bits (bits 6 and 7) of the preamble.

or (2) the external PTT input (SK4 pin 12 on the rear panel of the MA 1723).

or (3) when VOX is selected (bit 38 of word 3 set to a '1'), the presence of the audio modulation signal or the audio sidetone signal.

28. The transmit/receive condition is conveyed to the associated control unit via bit 32 of the revertive word 0 data ('1' for transmit, '0' for receive). Note that the application of a 0 V external mute signal to SK4 pin 7 on the rear panel overrides the transmit condition. Should a break occur in the SCORE data or SCORE clock signal for a period greater than approximately ten seconds (dependent upon baud rate), then the drive unit is muted and the fault bit (bit 33 of word 0) is set to a '1'.

Mute

29. When the mute condition is selected, the transmit state is inhibited, and bit 32 of the revertive word 0 data is set to zero.

Broadcast

30. The broadcast state is as given for the operate state (paras. 27 and 28) except that should a break occur in the SCORE data or SCORE clock signal, the conditions prevailing at the time of the break are maintained.

Tune

31. When tune is selected the MA 1723 generates a continuous carrier at the current operating frequency and at a preset level. Bit 32 of word 0 (the TRANSMIT bit) is set to a '1', provided external mute is not selected at the MA 1723.

High Power

32. Data bit 36 is normally set to the '1' high-power state, and is cleared to a '0' to select the low-power condition. This enables an internal drive level attenuator where the level of attenuation is controlled by a preset potentiometer.

Auto-Reset

33. Automatic reset is enabled by setting bit 37 to a '1'. Following a subsequent frequency change, and provided a successful frame comparison occurs, then the drive unit is automatically set to the mute condition, is retuned to the new frequency, and the mute condition is then removed. If the auto-reset bit is set to a '0' prior to a frequency change, then the drive unit is muted and the fault bit (word 0 bit 33) is set to a '1'.

VOX Transmission

34. When bit 38 is set to a '1' and the transmit/receive bits of the preamble (bits 6 and 7) are set to the receive condition, the VOX transmission circuit is enabled.

Low Power Select

35. In conjunction with the high power bit (36), if the associated linear amplifier has the facility to select different low power levels, bits 41 and 42 can be encoded to control the low power select lines on the MA 1723 (see table). If high power is selected, then bits 41 and 42 must be set to zero's.

BIT 36	BIT 41	BIT 42	STATE
0	0	0	MA1723 LOW POWER ONLY
0	1	0	LEVEL 1 (MA1723 is set to LOW POWER)
0	0	1	LEVEL 2 (MA1723 is set to LOW POWER)
1	0	0	HIGH POWER
1	1	X	ILLEGAL
1	X	1	ILLEGAL
0	1	1	ILLEGAL

User Functions

36. The last four bits of word 3 provide for the forward user functions where up to four earth (0 V) signals applied to the control unit are reproduced via the serial data at the drive unit. The four bits are labelled W, X, Y and Z and correspond with the similarly marked input and output connections of the control unit and drive unit respectively.

REVERTIVE DATA

37. The format for the revertive data is the same as for the control data so that essentially an inverse process takes place. Frame comparison however, does not take place and the revertive data is thus sent in single frames.

38. Provided that the control inhibit bit in the forward data preamble is not set to a '1' and that no errors occur in the control data, then the form of the revertive data is given by the following example:

Forward Data	WORD 0 MON	WORD 0 MON	WORD 1 FREQ	WORD 1 FREQ	WORD 3 MODE	WORD 3 MODE	
Resulting Revertive Data			WORD 0 MON	WORD 0 MON	WORD 1 FREQ	WORD 0 MON	WORD 3 MODE

39. In the above example, the forward data consists of two word 0 (monitor) frames, two word 1 (frequency) frames and two word 3 (mode) frames. Since two frames have to be sent and compared before any action may take place, the revertive data resulting from the forward data given in this example is shown lagging the forward data by two 48-bit words, or 96 bits. The contents of the two blank revertive data words are dependent on the previously sent control data.

40. The two forward monitor frames are compared and, since the two frames are the same, a monitor frame is sent back. The next frame comparison however, takes place between a monitor frame and a frequency frame. The frame comparison is therefore unsuccessful and, although an error does not exist, it is arranged to send back a monitor frame. Two frequency frames are now compared, and result in a revertive frequency frame. The next two frames, frequency and mode, result in a revertive monitor frame, two mode frames result in a revertive mode frame, and so on.

Frame Comparison Failure

41. A frame comparison error signal is generated only on the failure of three consecutive frame comparisons, as shown in the following example.

Frequency Data	WORD 0 MON	WORD 0 MON	WORD 1 FREQ	WORD 1 FREQ	WORD 3 MODE	WORD 3 MODE	
		ERROR					
Revertive Data			WORD 0 MON	WORD 0 MON	WORD 0 FREQ	WORD 0 MON	WORD 3 MODE
		ERROR INDICATION				BIT 34 SET	

42. In the above example, the forward data is the same as for the previous example except for a bit error in the first word 1 frequency frame. The two monitor frames result in a revertive monitor frame and the next two frames (monitor and frequency) result in a monitor frame as before. The two frequency frames are compared and this time, due to the bit error, the frame comparison is unsuccessful, resulting in a further revertive monitor frame. The next two frames (frequency and mode) being dissimilar also result in a revertive monitor frame. Thus three consecutive revertive monitor frames result following the FAILURE of three consecutive frame comparisons, and a frame comparison error signal is generated (i.e. bit 34 is set to a '1').

Control Inhibit

43. If the control inhibit bit (bit 8 of the preamble) in a forward control data frame is set to a '1', and provided that the return monitor bit (bit 9 of the preamble) is not set to a '1', then the revertive data frames are sent in pairs and in numerical sequence and convey the actual drive unit setting data.

Return Monitor

44. If the return monitor bit (bit 9 of the preamble) in a series of forward control data frames is set to a '1', then the revertive data consists of a series of continuous monitor frames.

CLOCK CIRCUITS

45. These provide the timing signals required by the various parts of the system. The basic data rate clock signal may be generated either by an external unit, such as a modem, or may be provided by an internal clock generator (7.8 kHz derived from the CPU clock).

SIGNAL-TO-LINE REQUIREMENTS

46. The signal-to-line requirements for the serial data and clock signals comply with CCITT Recommendation V10 (compatible with EIA RS 423). This specifies the electrical characteristics for unbalanced double-current interchange circuits for general use with integrated circuit equipment in the field of data communications. It is intended for use at the lower signalling rates only and its use should be avoided in the following cases:

(1) Where the interconnecting cable is too long for proper unbalanced circuit operation.

(2) Where extraneous noise sources make unbalanced circuit operation impossible.

(3) Where it is necessary to minimise interference with other signals.

47. The main V10 characteristics (as far as the MA 1723 is concerned) are summarised below:

(1) Binary 0 for data circuits, or ON for control and timing circuits, is defined as a voltage more positive than -3.0 V.

(2) Binary 1 for data circuits, or OFF for control and timing circuits, is defined as a voltage more negative than +0.3 V.

(3) Maximum Data Rate: 4.8 Kbit/s.

(4) Maximum Line Length: 1000 m at data rates up to 10 Kbit/s.

(5) Open circuit Driver Voltage: from $\pm$4 V to $\pm$6 V.

(6) Loaded Driver Voltage: equal to or greater than 0.9 times the open circuit driver voltage.

(7) Driver Output Load - Power Off: 100 microamperes (+0.25 V to -0.25 V).

(8) Driver Short-Circuit Current: $\pm$150 mA.

(9) Driver Slew Rate: Resistor controlled.

(10) Receiver Input Resistance: Equal to or greater than 4 Kilohms.

(11) Receiver Threshold: -0.2 V to +0.2 V.

(12) Maximum Receiver Input Voltage: $\pm$12 V.

SCORE INTERFACE BOARD

48. The SCORE interface board handles the transmission and reception of SCORE data between an MA 1723 drive unit and a suitable control unit (such as the Racal MA 1090). For a drive unit set to local control i.e. REMOTE not selected, control is via the front panel controls only, and revertive SCORE data is not produced. For a drive unit set to REMOTE control i.e. REMOTE selected at the front panel, the remaining front panel controls (except the LINE/SET/RF metering switch) are disabled, and the drive unit is under the control of an external control unit.

CIRCUIT DESCRIPTION (Fig. 14.1)

SCORE INTERRUPT

49. The software SCORE handling routine is initiated following the receipt by the processor board of a logic '0' interrupt signal from NAND gate G21. Since the unused Q6 output from latch ML8 is held at a '0', the resulting '1' from G17 enables NAND gate G20 for a '0' output from the interrupt latch ML17a, whilst the resulting '1' from G18 enables NAND gate G21 for the output from G21. Thus a '0' at the $\overline{Q}$ output of the interrupt latch ML17a is routed to the processor board via G20, G21 and PL45 pin 4 (para. 55)

CLOCK DETECTOR

50. The clock detector circuit comprises open-collector NAND gate G8, NAND gates G9, G10, G11, and two inverting buffers ML6d, ML6e. Its purpose is to detect the presence or absence of an externally applied clock signal (higher than approximately 300 Hz) and to allow the use of an internal SCORE clock signal only when the external clock signal is not present.

51. An externally applied SCORE clock signal (at SK38 pin 2) is routed via V10 line receiver ML1 to one input of G8 via invertr ML6a, and to the remaining input of G8 via delay components R11, C8. The resulting negative-going pulses at the output of G8 keep C9 discharged below the switching threshold of ML6d, producing a '1' at the output, which is applied to:

    (1) G9, to enable the external SCORE clock signal from ML1.

    (2) Inverter ML6e, to force a '1' at the output of G10 and so enable G11 for the external SCORE clock signal from G9.

52. If the external SCORE clock is removed (or falls below approximately 300 Hz), capacitor C9 is allowed to charge via R13, to the point where ML6d changes state. The resulting '0' output is inverted by ML6e to enable G10 for the internal SCORE clock signal at PL45 pin 5; it also forces a '1' at the output of G9 to enable G11 for the output signal from G10.

SYNC CODE DETECTOR

53. For a drive unit set to remote control, the SCORE control data, at SK38 pin 3, is applied via line receiver ML1 to a serial-to-parallel converter stage ML20 (para. 56) and via inverting buffer ML6c to the DA input of a dual 4-stage shift register ML15. The Q3A output from one section of the register is applied to the reset (RB) of the other section, where the data

input (DB) is connected to +5 V (logic '1'). Data is shifted into these registers on the positive-going transition of the SCORE clock signal from G11.

54. When an inverted sync. code is received, i.e. 1-0-0-0-0-0-X-X, it takes three clock pulses for the first '1' to reach the Q3A output; this holds the B section of the register in the reset state for the duration of the next clock pulse, and a further four clock pulses are required before the Q4B output changes to a '1' (Table 2). Thus the Q4B output of ML15 can only change to a '1' following the occurrence of five consecutive zeros at the DA input. This circuit does not detect the state of the last two bits of the received sync. code but this is subsequently checked by the system software. The '1' at the Q4B output of ML15 is applied to the clock input of the strobe pulse generator ML17b via glitch suppression components, R14, C10.

Table 2: Sync. Code Detector

SHIFT REGISTER STATES	1	2	3	4	5	6	7	8
Q1A	1	0	0	0	0	0	X	X
Q2A	X	1	0	0	0	0	0	X
Q3A	X	X	1	0	0	0	0	0
Q4A	X	X	0	1	0	0	0	0
Q1B	X	X	0	0	1	1	1	1
Q2B	X	X	0	0	0	1	1	1
Q3B	X	X	0	0	0	0	1	1
Q4B	X	X	0	0	0	0	0	1

X = 0 or 1

STROBE PULSE GENERATOR

55. The strobe pulse generator comprises D-type flip flop ML17b. When clocked by the output from the sync. code detector, the '1' at the D input is transferred to the Q output, the '0' at the $\overline{Q}$ output is applied to G12, and ML17b is thus reset on the next negative-going transition of the SCORE clock waveform from G11. The positive-going strobe pulse is applied to:

(1) One input of G14, which forms part of the output counter synchronisation circuit (para. 64).

(2) The strobe input of 8-bit shift and store register ML20 to load the internal storage latches with the first eight bits (the sync. code) of the received frame (para. 56).

(3) The reset input of an 8-bit BCD up-counter ML18a. This counter produces a positive-going pulse at the Q4 output for every eight SCORE clock cycles following reset, and these pulses are applied to the set input of ML17b to produce the strobe pulses for the remaining five bytes of the received data frame.

56. At the negative-going edge of each strobe pulse, the $\overline{Q}$ output of ML17b returns to a '1', and this clocks the SCORE interrupt latch ML17a. The resulting '0' at the $\overline{Q}$ output of ML17a is routed via G20 and G21 to the processor as an interrupt signal. The processor subsequently causes the production of a positive-going pulse at the Q1 output of address decoder stage ML19b (para. 67) to reset the interrupt latch and to output-enable the shift-and-store register ML20 (para. 56).

SERIAL-TO-PARALLEL CONVERTER

57. ML20 is an 8-stage serial shift register which has a storage latch associated with each stage. The data in each shift register stage is transferred to the storage register when a '1' is applied to the strobe (STB) input, and the stored data appears at the Q1 to Q8 parallel outputs when a '1' is applied to the enable (EN) input. When a '0' is present at the enable input, the Q1 to Q8 outputs are in the high-impedance 3-state condition.

PARALLEL-TO-SERIAL CONVERTER

58. The parallel-to-serial data converter comprises a pair of first in-first out (FIFO) registers ML14, ML11, and an 8-bit parallel or serial input/serial output shift register ML10. Each FIFO register is a 4-bits-wide by 16-bits-long storage device, and two such devices are used to produce an 8-bit-wide-by 16-bits-long register. The 4 x 16 data register in each device is under constant control of a logic network. Each word position in the array is clocked by a control flip-flop, which stores a marker bit; a '1' signifies an occupied position, whilst a '0' denotes a vacancy in that position. The control flip-flop detects the state of the preceding flip-flop and communicates its own status to the succeeding control flip-flop. When a control flip-flop is in the '0' state and detects a '1' in the preceding flip-flop, it generates a clock pulse which transfers data from the preceding four data latches into its own data latches, and resets the preceding control flip-flop to '0'. The first and last control flip-flops have buffered outputs, designated DIR (data in ready) and DOR (data out ready) respectively. Since all empty locations 'bubble' automatically to the input end, and all valid data ripples through to the output end, the status of the first control flip-flop (DIR) indicates if the FIFO is full, and the status of the last control flip-flop (DOR) indicates if the FIFO contains data. Since the earliest data (first in) is removed from the bottom of the stack (the output end), all subsequently entered data propagates (ripples) towards the output. Data is shifted into the FIFO on a positive-going transition at the shift-in (SI) pin provided the DIR output is at a '1' (the DIR output momentarily goes to a '0' when the data is shifted in, and remains at '0' should all 16-word locations be filled with valid data).

59. As soon as the first word entered has rippled to the output, the DOR output goes to a '1', and output data is latched at the Q outputs. The next word is latched at the output by a negative-going transition at the SO (shift out) input, and when this occurs, the DOR output momentarily goes to a '0'; R15 and C11 are included to prevent these momentary 0 V pulses affecting the operation of G19 and also to prevent the generation of spurious interrupts (via G18, G21). Data is loaded into the FIFO under software control (para. 63).

60. ML10 is an 8-stage parallel or serial input/serial output shift register. When the parallel/serial control input is at logic '1', data at the parallel input pins (from the FIFO registers) is loaded into the register synchronously with the positive transition of the clock signal. When the parallel/serial control input is at logic '0', data is serially shifted into and out of the register synchronously with the positive transition of the clock signal. Note that the falling edge of the parallel/serial pulse shifts out the next byte of data from the FIFO registers, and this data is loaded into ML10 by the next parallel/serial control pulse.

61. The parallel/serial control pulse from inverting NOR gate G22 is produced by ML12b, and occurs once every eight SCORE clock periods due to the action of the output counter ML18b. The operation of the circuit is as follows.

PARALLEL/SERIAL CONTROL SIGNAL

62. ML18b is a BCD up-counter which is clocked by the SCORE clock signal from G11. When a count of eight is reached, the Q4 output changes to a '1', the output from NOR gate G15 changes to a '0', and the resulting '1' output from G16 sets ML12b. The Q output of ML12b is thus set to a '1', and this is routed to:

(1) NAND gate G19; provided the FIFO is not empty (DOR is at '1'), then a '0' is applied to G22 and a positive transition occurs at the output.

(2) The clock input of ML12a; with a '0' at the D input, the $\overline{Q}$ output goes to a '1', G13 is enabled, and the '0' at the $\overline{Q}$ output of ML12b resets ML18b. The Q output of ML12a goes to a '0', and this maintains the '1' at the output of G15.

63. One-half SCORE clock period later, ML12b is clocked by the output from SCORE clock inverter ML6f, and the '0' at the D input causes the Q output to return to a '0'. Thus a positive-going output pulse is applied to the parallel/serial input of ML10 once every eight SCORE clock periods.

64. The loading of data into the FIFO register is under software control, and at the appropriate moment, the output counter ML18b is synchronised to the input counter ML18a by a start-in-sync. (SIS) signal from the address decoder (ML19a Q1 output). The action of the circuit is as follows.

65. Bytes of received SCORE control data from serial-to-parallel converter ML20 are routed to the processor board via the data bus and are temporarily stored in RAM. When a correct sync. code is recognised, a software counter is initialised and then counts successive bytes of the SCORE control data frame. When the last but one byte of the frame has been received, the start-in sync. pulse is applied to the set input of the start-in sync. (SIS) latch, and also to the reset input of ML12b, with the following results:

(1) The '0' at the $\overline{Q}$ output of ML12a forces a '1' at the output of NAND gate G13, and the output counter ML18b is held reset.

(2) The '1' at the Q output of ML12a enables NAND gate G15 for the next positive-going strobe pulse from ML17b.

(3) The '1' at $\overline{Q}$ output of ML12b is of no consequence at this point in the sequence.

(4) The '0' at the Q output of ML12b forces a '1' at the output of NAND gate G19, and the parallel/serial control input at ML10 pin 9 is held at a '0'.

66. A master reset signal (ML19a/Q2) is then applied to the FIFO register, and a sync. code is loaded in by the processor. When the last byte of the control data frame has been received, the data is processed, and the remaining bytes of the revertive data frame to be returned are loaded into the FIFO register. The strobe pulse from ML17b which loaded the last byte of the received frame into ML20 is also applied to the reset input of the input counter ML18a, and to NAND gate G14; since the remaining input of G15 is also at a '1', a '0' occurs at the output, and this forces a '1' at the output of G16. ML12b is thus set, and is clocked one-half SCORE clock period later by the output from ML6f. The resulting positive-going pulse at the Q output of ML12b results in a positive-going pulse at the output of G22, and the previously loaded sync. code (which has rippled through to the output of the FIFO register) is parallel-loaded into the output shift register ML10.

67. At the same time, the positive-going pulse at the Q output of ML12b clocks ML12a, the '0' at the D input results in a '1' at the $\overline{Q}$ output, and this removes the reset from ML18b (via G13). The '0' at the Q output of ML12a forces a '1' at the output of G14, and this enables G16 for subsequent '1' outputs from G15. The input and output counters, ML18a and ML18b respectively, are now synchronised, and this ensures synchronism between input and output SCORE data frames.

ADDRESS DECODER

68. The address decoder comprises a dual binary to 1-of-4 decoder ML19a, ML19b, and two NAND gates G1, G2. It decodes the levels present on the PA7, PA6, PA1 and PA0 address bus lines to produce, coincident with the strobe input (PL45 pin 9), one of six strobe output signals (B0 to B3, 70 and 71) as given in Table 3. Although the strobe addresses given are dedicated, because the PA2, PA3, PA4 and PA5 lines are not decoded, they are not uniquely defined.

Table 3: Address Decoder

ADDRESS									OUTPUT STROBE FUNCTION
HEX	7	6	5	4	3	2	1	0	
70	0	1	1	1	0	0	0	0	USER FUNCTIONS IN ENABLE
71	0	1	1	1	0	0	0	1	SCORE DATA IN ENABLE
B0	1	0	1	1	0	0	0	0	USER FUNCTIONS OUT ENABLE
B1	1	0	1	1	0	0	0	1	START IN SYNC (SIS)
B2	1	0	1	1	0	0	1	0	MASTER RESET (MR)
B3	1	0	1	1	0	0	1	1	SCORE DATA OUT

USER FUNCTIONS

69. The user function data from the associated control unit, conveyed by SCORE word 3, is routed by the processor and data bus to hex D-type latch ML8; this latch is then clocked by the QO output from ML19a (responding to address BO), and the user function data is routed via open-collector transistors TR1 to TR4 to the appropriate pins of rear panel connector SK5. The revertive user function data (conveyed by SCORE word 0) is applied to the appropriate pins of rear panel connector SK5 and is then routed to the processor via open-collector NAND gates G3 to G6 and data bus lines DO to D3 (by the application of address 70 to the address decoder).

SCORE INTERFACE BOARD (ST 82458)

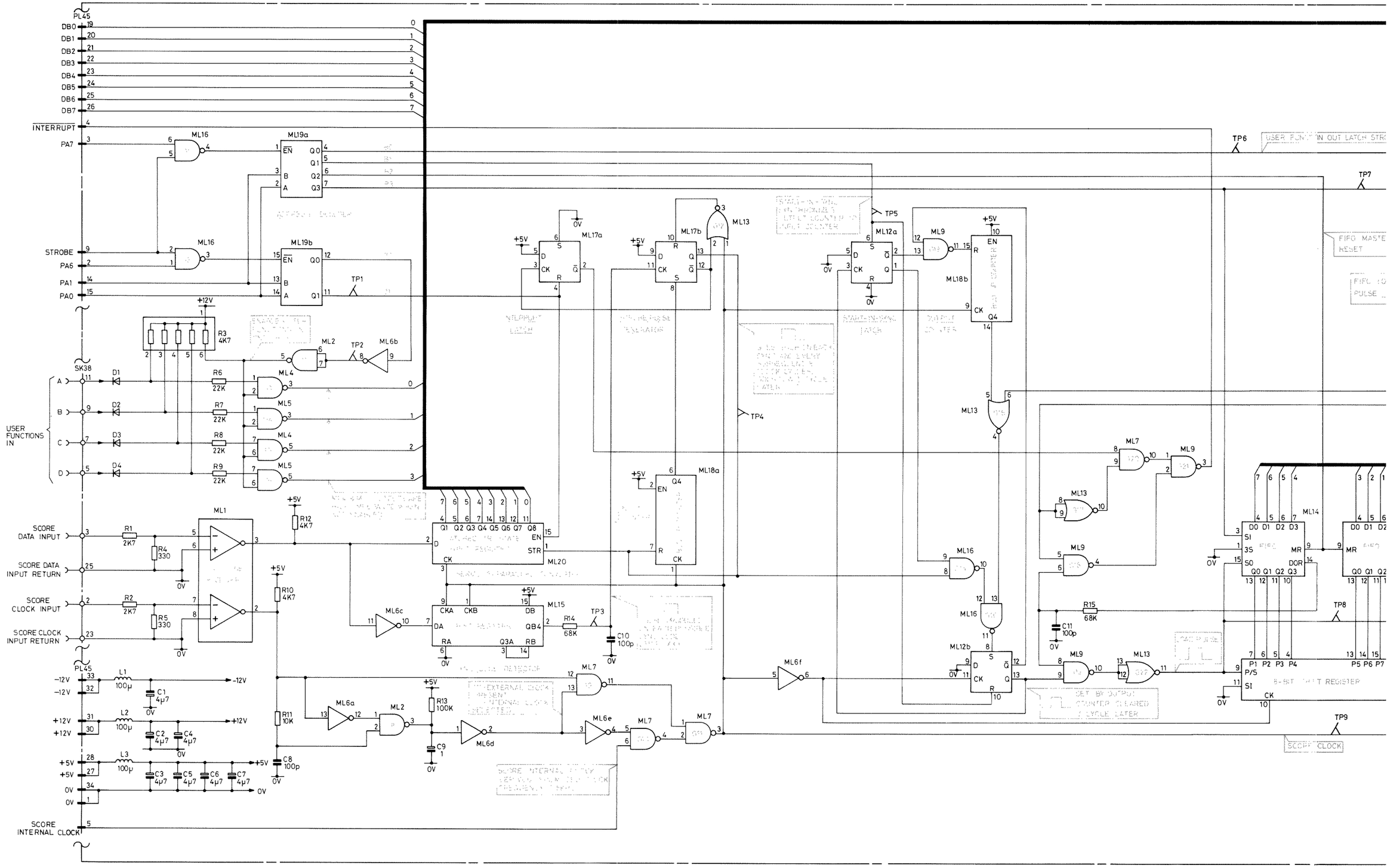
Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Resistors					
R1	2k7	Metal Oxide		2	916548
R2	2k7	Metal Oxide		2	916548
R3	4k7	5-resistor SIL Network		2	939649
R4	330	Metal Oxide		2	915690
R5	330	Metal Oxide		2	915690
R6	22k	Metal Oxide		2	913493
R7	22k	Metal Oxide		2	913493
R8	22k	Metal Oxide		2	913493
R9	22k	Metal Oxide		2	913493
R10	4k7	Metal Oxide		2	913490
R11	10k	Metal Oxide		2	914042
R12	4k7	Metal Oxide		2	913490
R13	100k	Metal Oxide		2	915190
R14	68k	Metal Oxide		2	916478
R15	68k	Metal Oxide		2	916478
R16	22k	5-resistor SIL Network		2	938324
R17	270k	Metal Oxide		2	923598
R18	10k	Metal Oxide		2	914042
R19	10k	Metal Oxide		2	914042
R20	10k	Metal Oxide		2	914042
R21	10k	Metal Oxide		2	914042
Capacitors			V		
C1	4µ7	Tantalum Bead	35	20	914026
C2	4µ7	Tantalum Bead	35	20	914026
C3	4µ7	Tantalum Bead	35	20	914026
C4	4µ7	Tantalum Bead	35	20	914026
C5	4µ7	Tantalum Bead	35	20	914026
C6	4µ7	Tantalum Bead	35	20	914026
C7	4µ7	Tantalum Bead	35	20	914026
C8	100p	Ceramic Disc	500	10	917417
C9	1µ0	Tantalum Bead	35	20	923571
C10	100p	Ceramic Disc	500	10	917417
C11	100p	Ceramic Disc	500	10	917417

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Inductors					
L1	100µH	Choke		10	939161
L2	100µH	Choke		10	939161
L3	100µH	Choke		10	939161
Connectors					
PL45		Plug, 34-way			939991
SK38		Cable Assembly			BA82563/2
		Comprising:			
		Socket, 34-way			934821
		Connector, PCB, 34-way			940000
		Cable, flat, 34-way			931531
		Clamp, Strain relief, 34-way			934812
Diodes					
D1-D4		Silicon 1N4149			923222
Transistors					
TR1-TR4		NPN Silicon 2N2222A			923217
Integrated Circuits					
ML1		Line Receiver 9637ATC			939908
ML2		Dual 2-input NAND Buffer 40107			931052
ML3		Line Driver 9636ATC			939907
ML4		Dual 2-input NAND Buffer 40107			931052
ML5		Dual 2-input NAND Buffer 40107			931052
ML6		Hex Inverter 4069			930999
ML7		Quad 2-input NAND gate 4011			930028
ML8		Hex D-type Flip-Flop 40174			931060
ML9		Quad 2-input NAND gate 4011			930028
ML10		8-bit Shift Register 4014			930972

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
ML11		FIFO Register 40105			931050
ML12		Dual D-type Flip-Flop 4013			926860
ML13		Quad 2-input NOR gate 4001			930027
ML14		FIFO Register 40105			931050
ML15		Dual 4-bit Shift Register 4015			930973
ML16		Quad 2-input NAND gate 4011			930028
ML17		Dual D-type Flip-Flop 4013			926860
ML18		Dual BCD Up-Counter 4518			928002
ML19		Dual binary to 1-of-4 decoder 4555			928189
ML20		8-bit Shift Register 4094			929324

Miscellaneous

		Captive Fastener			939306
		8-pin DIL IC Socket			939604
		14-pin DIL IC Socket			930605
		16-pin DIL IC Socket			930606
		Test Point			936148



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TH3071	DC81657	14.1
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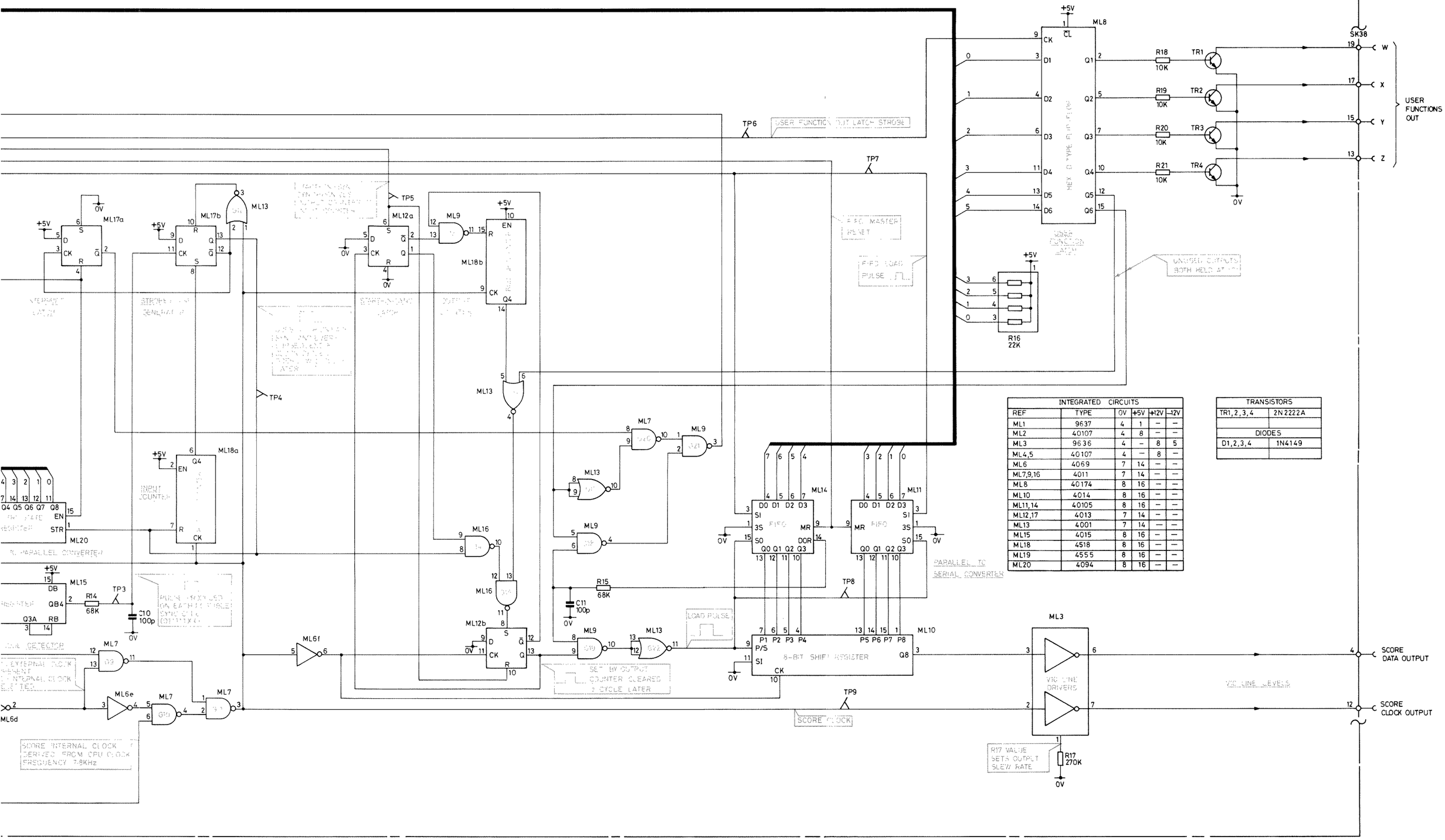
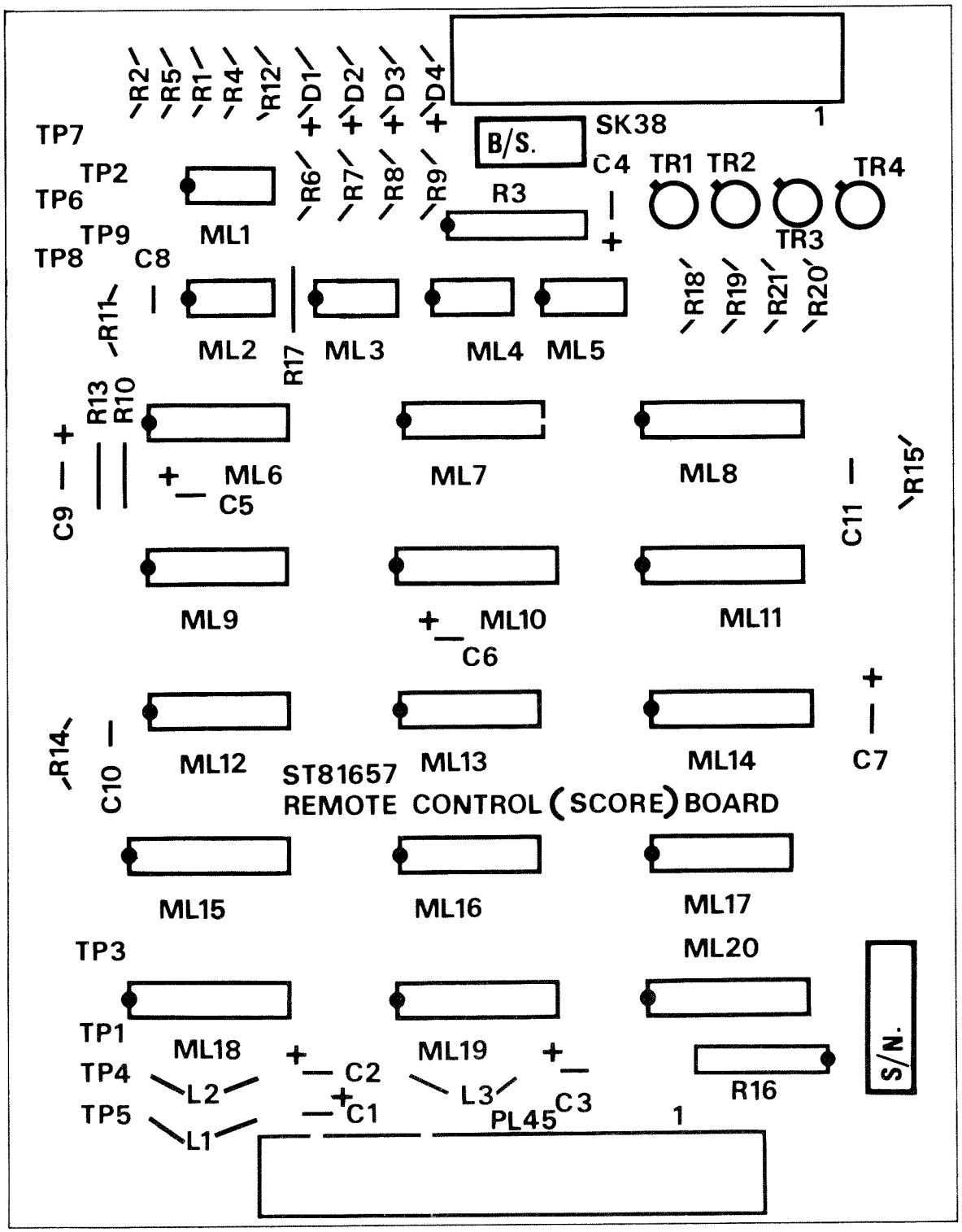


INTEGRATED CIRCUITS					
REF	TYPE	0V	+5V	+12V	-12V
ML1	9637	4	1	–	–
ML2	40107	4	8	–	–
ML3	9636	4	–	8	5
ML4,5	40107	4	–	8	–
ML6	4069	7	14	–	–
ML7,9,16	4011	7	14	–	–
ML8	40174	8	16	–	–
ML10	4014	8	16	–	–
ML11,14	40105	8	16	–	–
ML12,17	4013	7	14	–	–
ML13	4001	7	14	–	–
ML15	4015	8	16	–	–
ML18	4518	8	16	–	–
ML19	4555	8	16	–	–
ML20	4094	8	16	–	–

TRANSISTORS	
TR1,2,3,4	2N2222A
DIODES	
D1,2,3,4	1N4149

Circuit: SCORE Interface Board

Fig.14.1



RACAL

TH 3071	DA 81656/4
1	

Layout : SCORE Interface Board

Fig.14.2

CHAPTER 15

FSK BOARD

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Illustrations

CHAPTER 15

FSK BOARD

INTRODUCTION

1. The optional FSK board accepts polar (double current), negative/neutral or positive/neutral telegraph signals (selection via link LK1) and produces a tone shift keyed (TSK) output signal, about a nominal 2 kHz centre frequency. The frequency shift may be adjusted over the range plus and minus 42 Hz to plus and minus 425 Hz, using an internal preset control.

CIRCUIT DESCRIPTION (Fig. 15.1)

2. The telegraph input stage TR1, LK1, ML2, can accept single or double current signals over the voltage range 5 V-0-5 V and 80 V-0-80V. With a '0' at the FSK TEST input (from the processor via the front panel interface board), a '0' is also present at the open-collector comparator ML3a. Exclusive OR gate ML2b thus acts as a non-inverting buffer for the inverted telegraph output from TR1, whilst inverting exclusive OR gate ML2a caters for the NORMAL output.

3. Transistors TR2 to TR5 and C2 shape the keyed input signal to trapezoidal form, with rise and fall times of approximately 750 microseconds. The output voltage at TP2 is then applied via shift level control R15 and current source stage ML3c, TR6, to a nominal 8 kHz voltage controlled oscillator ML3d.

4. With no applied telegraph signal (at SK46 pin 8), the setting of the current source resistor R20 determines the charging time constant for capacitor C4, and hence the frequency of the square wave output from voltage comparator ML3d, at TP5 (to set the centre frequency, LK2 is removed and R20 is set for a TSK output frequency (at TP6) of exactly 2 kHz). When the telegraph signal is subsequently applied, the current source transistor TR6, and hence the oscillator frequency, is controlled by the voltage applied to the non-inverting input of ML3c.

5. The output signal from ML3d is buffered and divided by four dual D-type flip-flop M4a, ML4b, and R28 is adjusted for a TSK output signal level of approximately 50 mV peak.

6. The 0 V FSK FITTED signal, which is automatically produced when the optional FSK board is installed into the drive unit, is routed to the processor board via the front panel interface board. The FSK INHIBIT signal is routed from the processor board and via the front panel interface board. When FSK is not selected, the open-collector output of ML3b is pulled up to +12 V (via R11), and the reset condition is applied to ML4b to inhibit the TSK output.

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number

FSK BOARD (ST82356)

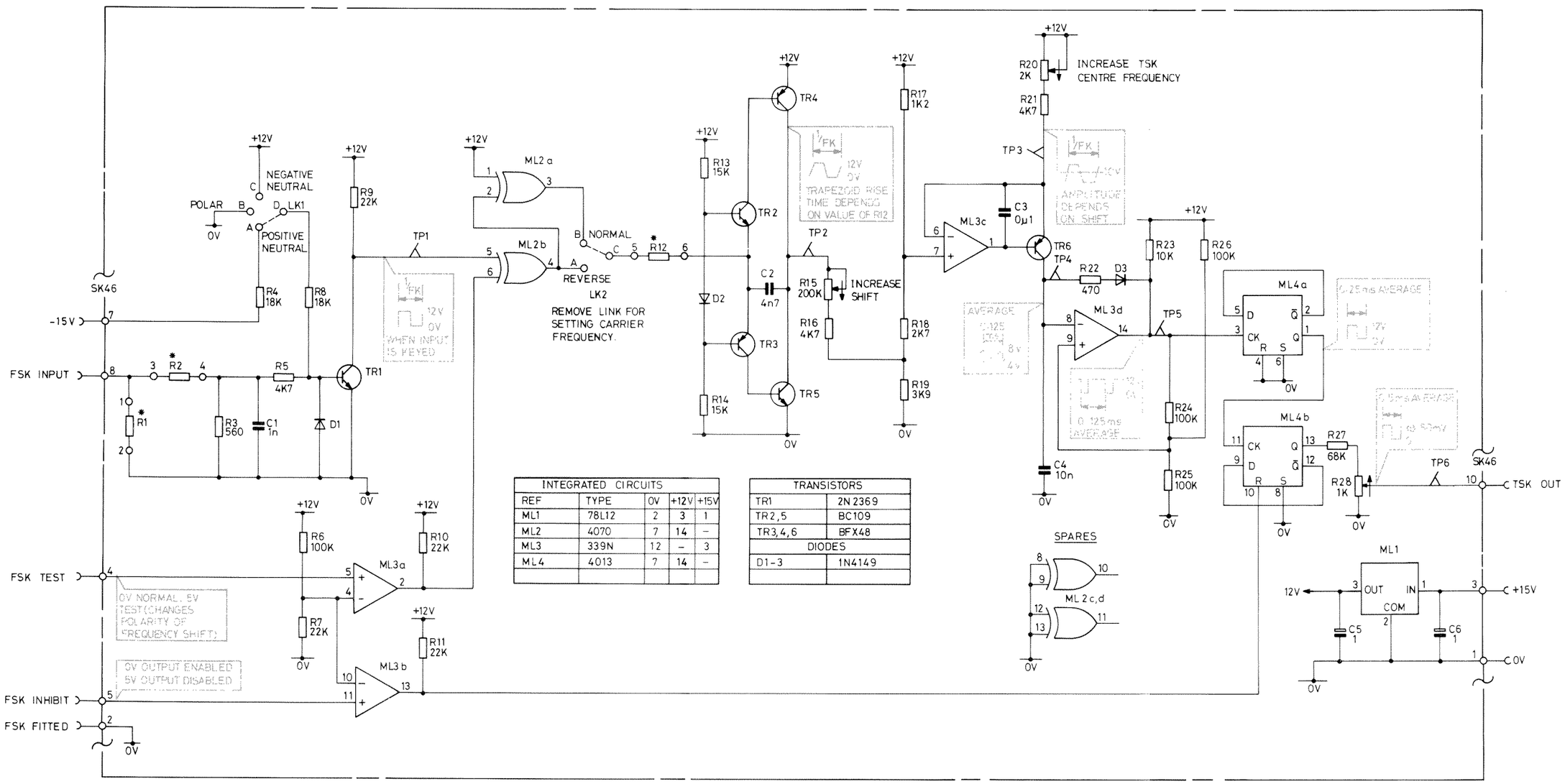
Resistors

R1	Value dependent on output voltage and designated working current			
R2	of teleprinter. See Chap. 2.			
R3	560	Metal oxide	2	917061
R4	18k	Metal oxide	2	900994
R5	4k7	Metal oxide	2	913490
R6	100k	Metal oxide	2	915190
R7	22k	Metal oxide	2	913493
R8	18k	Metal oxide	2	900994
R9	22k	Metal oxide	2	913493
R10	22k	Metal oxide	2	913493
R11	22k	Metal oxide	2	913493
R12	100k	Metal oxide	2	915190
R13	15k	Metal oxide	2	920645
R14	15k	Metal oxide	2	920645
R15	200k	Metal oxide	2	939917
R16	4k7	Metal oxide	2	913490
R17	1k2	Metal oxide	2	911179
R18	2k7	Metal oxide	2	916548
R19	3k9	Metal oxide	2	915074
R20	2k	Variable, preset	10	934265
R21	4k7	Metal oxide	2	913490
R22	470	Metal oxide	2	920758
R23	10k	Metal oxide	2	914042
R24	100k	Metal oxide	2	915190
R25	100k	Metal oxide	2	915190
R26	100k	Metal oxide	2	915190
R27	68k	Metal oxide	2	916478
R28	1k	Variable, preset	20	920315

Capacitors

			Volts		
C1	1n	Ceramic disc	500	20	915243
C2	4n7	Ceramic Plate	100	5	940044
C3	0µ1	Polycarbonate	100	10	931130
C4	10n	Polycarbonate	400	10	931136
C5	1µ0	Tantalum Bead	35	20	923571
C6	1µ0	Tantalum Bead	35	20	923571

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Connectors					
SK46		Cable assembly			BA82571
		comprising:			
		Socket, 10-way			932863
		Connector, PCB, 10-way			932863
		Cable, flat, 10-way			931526
		Clamp, strain relief, 10-way			934807
Diodes					
D1		Silicon 1N4149			923222
D2		Silicon 1N4149			923222
D3		Silicon 1N4149			923222
Transistors					
TR1		NPN Silicon 2N2369			906842
TR2		NPN Silicon BC109			923234
TR3		PNP Silicon BFX48			915231
TR4		PNP Silicon BFX48			915231
TR5		NPN Silicon BC109			923234
TR6		PNP Silicon BFX48			915231
Integrated Circuits					
ML1		+12 V Regulator 78L12			938455
ML2		Quad Exclusive OR gate	4070		930856
ML3		Quad Comparator 339			925952
ML4		Dual D-type flip-flop	4013		926860
Miscellaneous					
LK1,LK2		Link, Shorting			927090
		14-pin DIL IC socket			930605
		Test Point			936148
		Captive Fastener			930396



INTEGRATED CIRCUITS				
REF	TYPE	0V	+12V	+15V
ML1	78L12	2	3	1
ML2	4070	7	14	–
ML3	339N	12	–	3
ML4	4013	7	14	–

TRANSISTORS	
TR1	2N2369
TR2,5	BC109
TR3,4,6	BFX48
DIODES	
D1-3	1N4149

* THE VALUES OF R1 & R2 ARE DEPENDANT ON THE OUTPUT VOLTAGE AND DESIGNATED WORKING CURRENT OF TELEPRINTER. THE VALUE OF R12 IS SELECTED FOR OPTIMUM ENVELOPE SHAPING FOR A SPECIFIED BAUD RATE. NORMALLY 100K FITTED FOR 100 BAUDS.

RACAL

TH3071	DC82356	15-1	1/2
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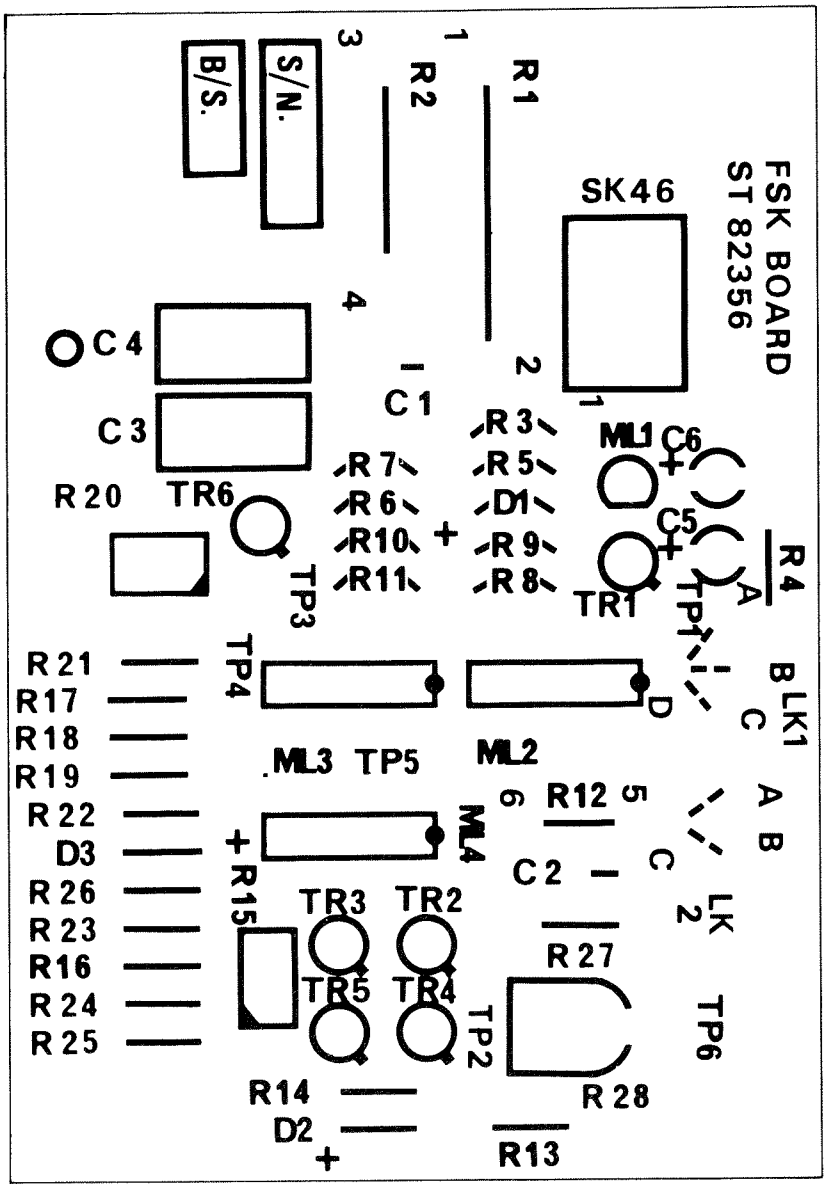
TH3071 DC82356 15-1 2/2

Circuit : FSK Board

Fig. 15-1



RACAL

TH 3071	CA 82355/4
1	

Layout: FSK Board

Fig.15.2

CHAPTER 16

FREQUENCY STANDARD

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CHAPTER 16

FREQUENCY STANDARD

INTRODUCTION

1. One of two types of 5 MHz frequency standard may be fitted to the drive unit (dependent upon the degree of frequency stability required) as an option. The two types of frequency standard are described below. Note that either type may be retrospectively fitted to a unit by ordering the appropriate kit of parts (ST 82651 for the 9420 kit, ST 82650 for the 9442 kit).

FREQUENCY STANDARD TYPE 9442 (Fig. 16.1)

2. The Racal 9442 frequency standard is a fast warm-up crystal oscillator of small physical size which provides a high degree of accuracy and long term stability with low power consumption (Table 1). The crystal is housed in a temperature controlled oven which, together with the maintaining circuit and a buffer amplifier, is fitted in a metal can with polyurethane foam to provide heat insulation. Access may be gained to the internal trimmer capacitor after removal of a small rubber plug. Adjustment procedures are given in Chap. 19. Connections are made via a B7G base, with pin connections as given in Table 2.

FREQUENCY STANDARD TYPE 9420 (Fig. 16.2)

3. The Racal 9420 frequency standard is a compact crystal oscillator similar in construction to the 9442. It contains a high-quality crystal which is operated in the third overtone mode. Like the 9442, the metal can contains polyurethane foam for heat insulation and a removeable rubber plug allows access to the internal multi-turn trimmer capacitor. For finer adjustment, a potentiometer is fitted to the frequency standard assembly which sets the voltage applied to an internal varactor diode. Adjustment instructions are given in Chap. 19. Pin connections are given in Table 3.

Table 1: Frequency Standard Specifications

	UNITS	9442	9420
Frequency	MHz	5	5
Daily Ageing Rate on Delivery		1×10^{-8}	2×10^{-9}
Daily Ageing Rate after 3 months		3×10^{-9}	5×10^{-10}
Short Term Stability over 1 Second		5×10^{-10}	1×10^{-10}
Warm-up time for 1×10^{-7} accuracy	Minutes	4	20
Retrace Characteristics		4×10^{-8} in 24 hours	2×10^{-8} in 24 hours
Temperature Operating Range	^{o}C	-10 to +60	-10 to +60
Stability with Temperature Change	Per ^{o}C	3×10^{-9}	6×10^{-10}
Stability with supply voltage change	For 10% change	4×10^{-8}	5×10^{-9}
Minimum Output Level	mV r.m.s.	250 into 50 Ω	250 into 50 Ω
Trim Range		-6 +3 parts in 10^6	-8 +2 parts in 10^7
Supply Voltage	V	12	12
Typical Supply Current at $25^{o}C$	mA	60	120
Size	cm in	5 x 5 x 5 2 x 2 x 2	5 x 5 x 9.5 2 x 2 x 3.75
Base		B7G	B7G

Table 2: 9442 Pin Connections

1	5 MHz Output relative to pin 7
2	Not used
3	Not used
4	+12 V supply
5	Not used
6	Not used
7	0 V (also connected to can)

Table 3: 9420 Pin Connections

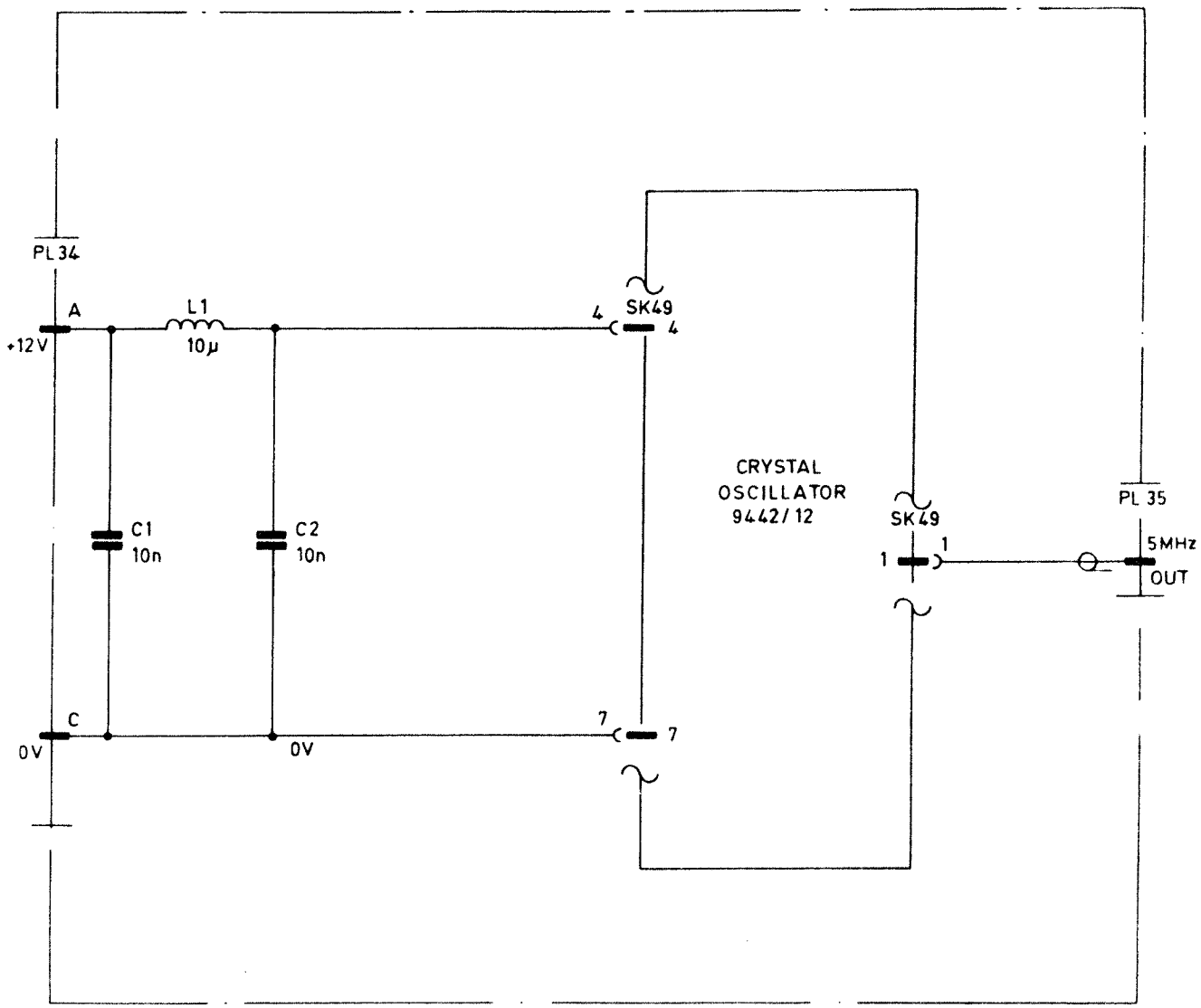
1	5 MHz Output relative to pin 7
2	Internally stabilised +5.6 V varactor diode control voltage
3	+7.5 V stabilised monitor output
4	+12 V supply
5	Internally stabilised +2.8 V output
6	Varactor diode connection
7	0 V (also connected to can)

REPAIR

4. If the specified performance of either type of frequency standard cannot be obtained, users are advised to return the faulty module to Racal Communications Limited for servicing, since select-on-test components and precise assembly techniques are employed to ensure the specified performance.

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
		9442 FREQUENCY STANDARD ASSEMBLY (ST82851)			
Capacitors					
C1	10n	Ceramic Disc	250	+40 -20	900067
C2	10n	Ceramic Disc	250	+40 -20	900067
Inductors					
L1	10µH	Choke		10	922364
Connectors					
PL34		Plug			938471
PL35		Plug, Coaxial			916499
SK49		Socket, B7G			938473
Miscellaneous					
		9442 Frequency Standard			933706
		Captive Screw			AD80541

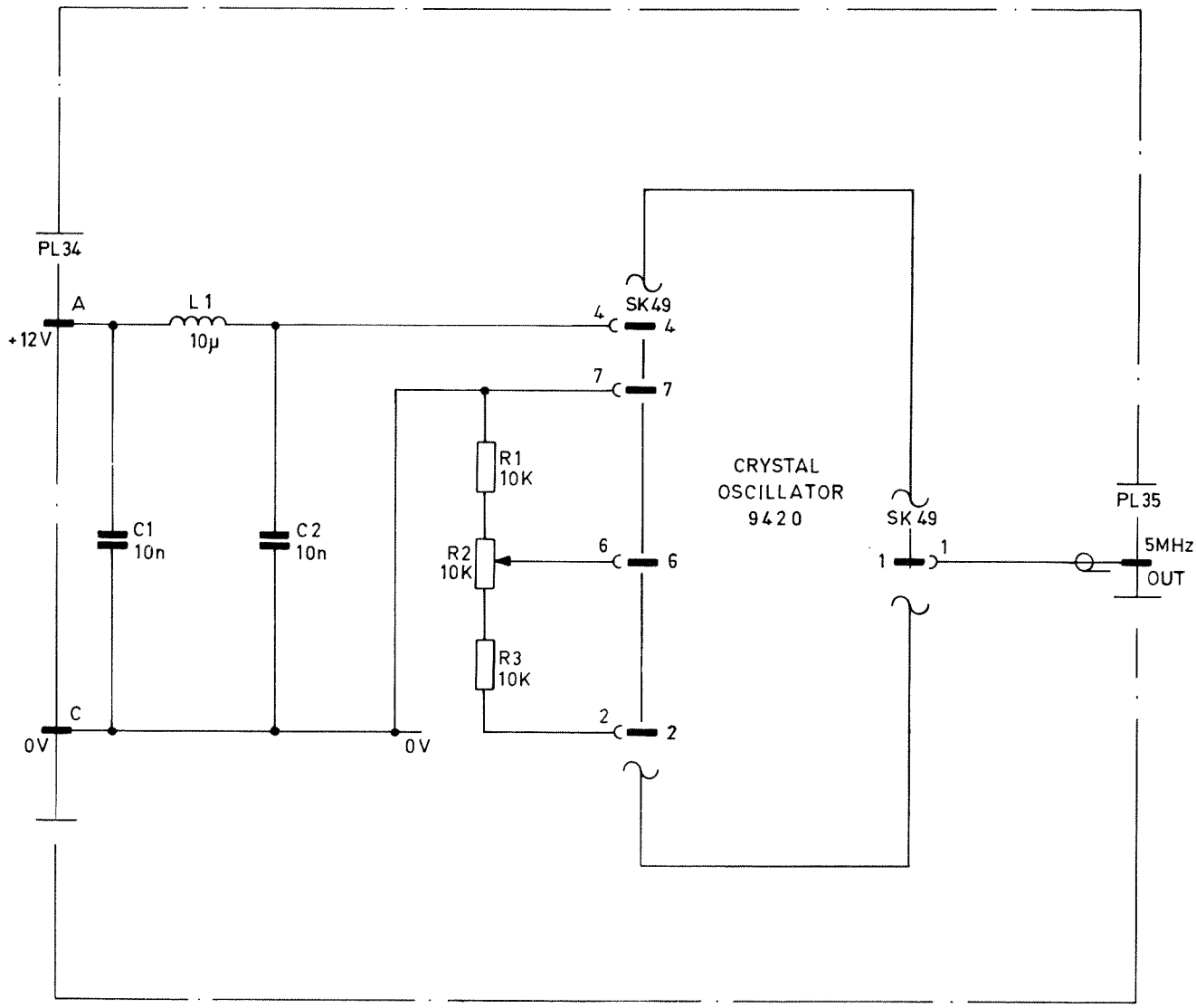
Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
		9420 FREQUENCY STANDARD ASSEMBLY (ST82852)			
Resistors					
R1	10k	Metal oxide		2	914042
R2	10k	Variable, preset		10	920730
R3	10k	Metal oxide		2	914042
Capacitors					
C1	10n	Ceramic Disc	250	+40 -20	916187
C2	10n	Ceramic Disc	250	+40 -20	916187
Inductor					
L1	10µH	Choke		10	922364
Connectors					
PL34		Plug			938471
PL35		Plug, Coaxial			916499
SK49		Socket, B7G			938473
Miscellaneous					
		9420 Frequency Standard			921601
		Captive Screw			AD80541
		Potentiometer Lock			906368



RACAL

TH 3071	BC82851
1	

Circuit : 9442 Frequency Standard Assembly Fig.16.1



RACAL

TH 3071	BC 82852
1	

Circuit : 9420 Frequency Standard Assembly

Fig.16.2

CHAPTER 17

INTERCONNECTIONS

CONTENTS

Illustrations

CHAPTER 17

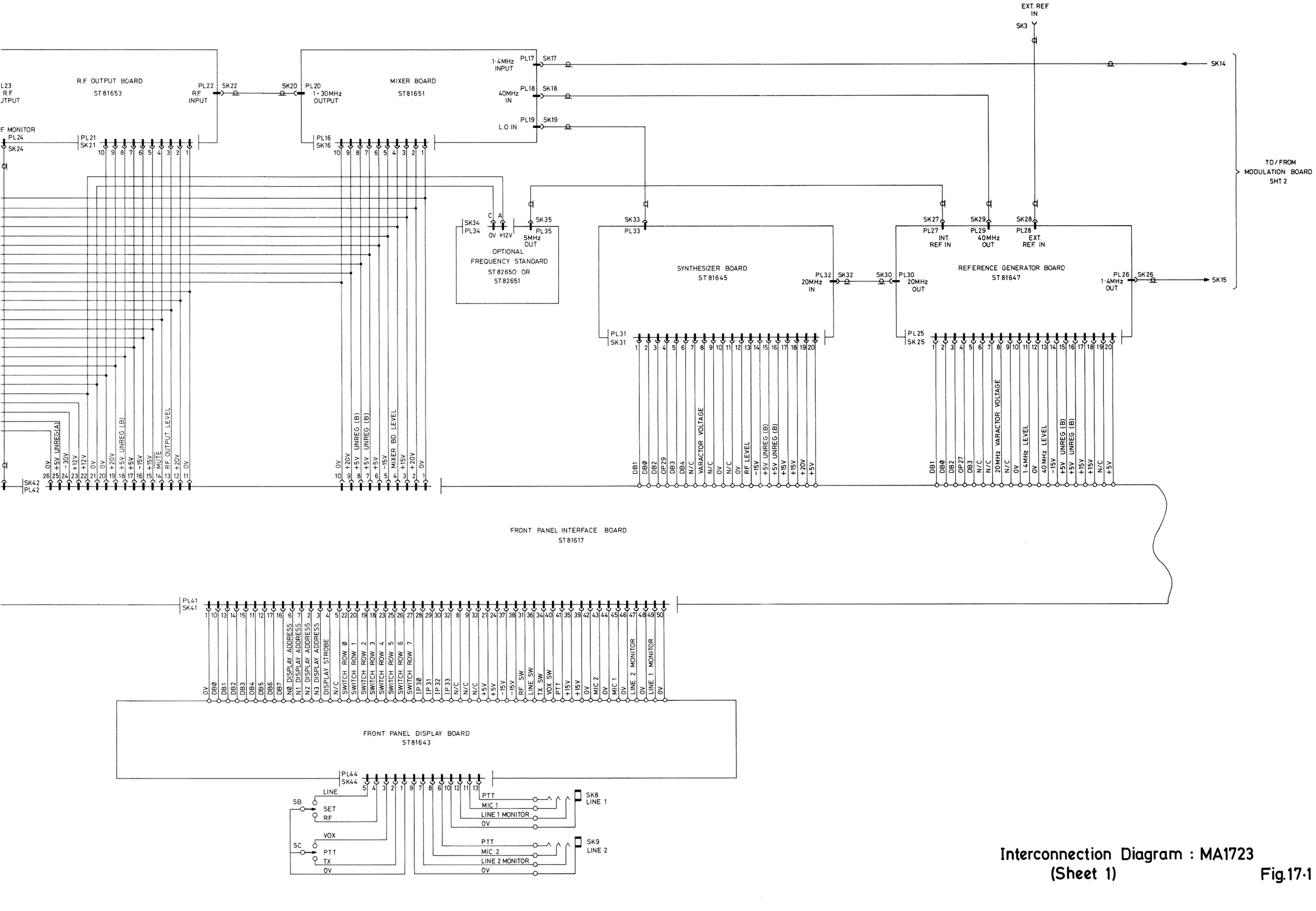
INTERCONNECTIONS

INTRODUCTION

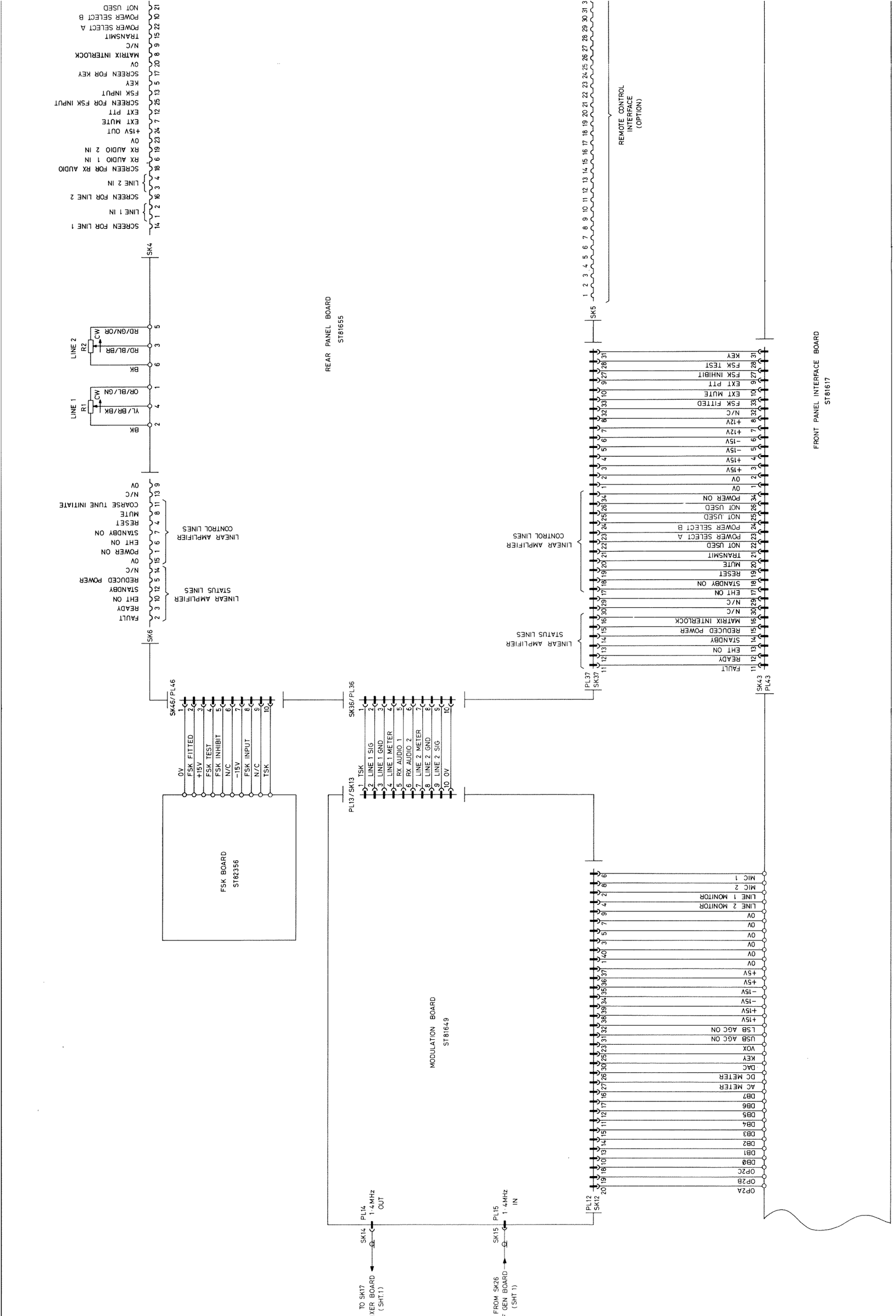
1. This chapter contains the overall unit interconnection diagram, which is given on two sheets (Figs. 17.1 and 17.2). The external connection multi-way sockets form part of the rear panel board and are given in Fig. 17.2. Refer to Chapter 2 for further rear panel connection information. For details of chassis mounted components and internal interconnecting cable assemblies, refer to Chapter 21.

R.F OUT
SK2
SK23
PL23
R.F
OUTPUT
R.F OUTPUT BOARD
ST 81653
PL22
R.F
INPUT
SK22
SK20
PL20
1-30MHz
OUTPUT
MIXER BOARD
ST81651
1·4MHz
INPUT
PL17
SK17
40MHz
IN
PL18
SK18
L.O. IN
PL19
SK19
R.F MONITOR
PL24
SK24
PL21
SK21
PL16
SK16
PL10/SK10
POWER SUPPLY
MODULE
ST80548
PL1
L
N
E
SK11
PL11
B
A
D
E
C
POWER
SA
SK47
PL47
SK42
PL42
0V
+5V UNREG(A)
-30V
+12V
+12V
0V
0V
+20V
+5V UNREG (B)
+5V
-15V
+15V
MUTE
RF OUTPUT LEVEL
+20V
0V
0V
+20V
+5V UNREG (B)
+5V UNREG (B)
+5V
-15V
MIXER BD LEVEL
+15V
+20V
0V
SK34
PL34
C
A
0V
+12V
SK35
PL35
5MHz
OUT
OPTIONAL
FREQUENCY STANDARD
ST 82650 OR
ST 82651
SK33
PL33
SYNTHESIZER BOARD
ST 81645
PL
20MHz
IN
PL31
SK31
DB1
DB0
DB2
OP29
DB3
DB4
N/C
VARACTOR VOLTAGE
N/C
0V
N/C
0V
RF LEVEL
-15V
+5V UNREG (B)
+5V UNREG (B)
+15V
+15V
+20V
+5V
FRONT PANEL INTERFACE BOARD
ST 81617
RF
(FRONT PANEL)
SK7
SK48
PL48
PL41
SK41
0V
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
N0 DISPLAY ADDRESS
N1 DISPLAY ADDRESS
N2 DISPLAY ADDRESS
N3 DISPLAY ADDRESS
DISPLAY STROBE
N/C
SWITCH ROW 0
SWITCH ROW 1
SWITCH ROW 2
SWITCH ROW 3
SWITCH ROW 4
SWITCH ROW 5
SWITCH ROW 6
SWITCH ROW 7
IP 30
IP 31
IP 32
IP 33
N/C
N/C
+5V
+5V
-15V
RF SW
LINE SW
TX SW
VOX SW
PTT
+15V
+15V
0V
MIC 2
0V
MIC 1
0V
LINE 2 MONITOR
0V
LINE 1 MONITOR
0V
FRONT PANEL DISPLAY BOARD
ST81643
PL44
SK44
LINE
SB
SET
RF
VOX
SC
PTT
TX
0V
PTT
MIC 1
LINE 1 MONITOR
0V
SK8
LINE 1
PTT
MIC 2
LINE 2 MONITOR
0V
SK9
LINE 2

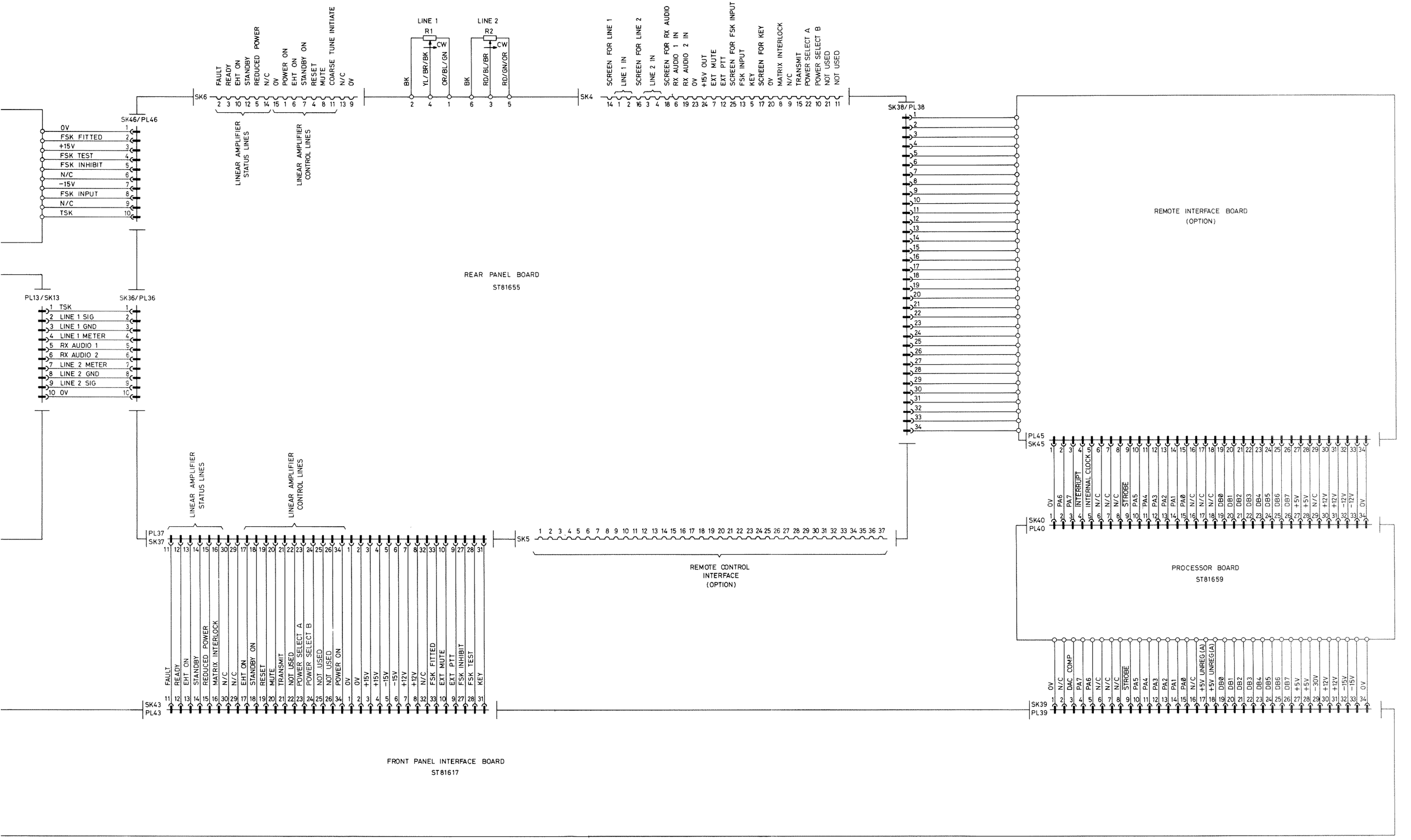
RACAL
TH3071 OC82642
2



Interconnection Diagram : MA1723
(Sheet 1) **Fig.17·1**



RACAL
TH3071 | DC82642
2



Interconnection Diagram : MA1723
(Sheet 2)

Fig.17-2

CHAPTER 18

SELF-TEST ROUTINES

CONTENTS

Tables

CHAPTER 18

SELF-TEST ROUTINES

INTRODUCTION

1. The MA1723 contains a number of built-in test routines (stored in ROM) which may be used as part of a functional test procedure (as detailed in Chap. 19) and also to assist in the location of a fault (Chap. 20). This chapter describes the test routines, provides an interpretation of the test results when a failure is detected, and refers the reader to the associated manual tests given in Chap. 20 to localise a faulty assembly or component. The routines, commonly referred to as BITE (built-in test equipment), are described firstly in the form of a tabulated flow chart, and then each routine is described in detail.

2. To enter the self-test mode, the REM pushbutton is held depressed whilst the two-digit test number (00 to 21) is entered. The REM pushbutton is then released to start the test. If the routines are started at test number 00, then tests 00 to 06 are carried out automatically and in sequence (assuming no fault is detected). To continue with the test routines test number 07 is entered, and routines 07 to 15 are then carried out and in sequence. At certain points during this sequence of operation, the test number flashes on and off to indicate that operator intervention is required. The last six test routines (numbers 16 to 21) must be individually selected.

3. To exit from the self-test mode, at any time, press and release the RCL pushbutton. A prior condition exists for test number 07 (front panel switch test) in that the number displayed at the frequency position must be 03 or higher before the exit can be achieved (see para. 17). If,during any self-test routine, the exit condition is not achieved by pressing and releasing RCL, set the POWER switch to OFF, and then back to ON. The test routine currently being executed can be restarted at any time by pressing and releasing the REM pushbutton. When a fault is detected, the test sequence stops and a fault code may be displayed. The test sequence may however, be continued by pressing and releasing the ENTER pushbutton.

   NOTE: All audio key or FSK inputs must be removed from the unit before carrying out the self-test routines.

4. The following flow chart refers to reader (when a fault is detected) to the appropriate manual tests contained in Chapter 20. The number of the manual test, preceded by the letter M, is the same as the self-test routine number.

SELF-TEST ROUTINE FLOWCHART

STEP 1	TEST	Press and hold the REM pushbutton, then enter 00. Does 00 appear in the CHANNEL display?
Action		YES: Step 2 NO: Test M00/a

STEP 2	00 POWER SUPPLIES	Release REM pushbutton. Does CHANNEL display change to 01?
Action		YES: Step 3 NO: Step 23

STEP 3	01 ROM TEST	Has a fault code (failed ROM device PD number) appeared in the frequency display?
Action		NO: Step 4 YES: Test M01 - ROM sum incorrect

STEP 4	02 RAM TEST 1	Any MODE legends displayed?
Action		NO: Step 5 YES: Test M02 - address or data bus fault

STEP 5	03 RAM TEST 2	Any MODE legend displayed?
Action		NO: Step 6 YES: Test M03 - RAM fault

STEP 6	04 EAROM TEST	Any MODE legends displayed?
Action		NO: Step 7 YES: Test M04 - EAROM fault
	SEE NOTE	

STEP 7	05 I/O BUS TEST	Any meter segment displayed?
Action		NO: Step 8 YES: Test M05 - I/O Bus Fault

STEP 8	06 DISPLAY TEST	Is the display visibly faulty?
Action		NO: Step 9 YES: Test M06

STEP 9	07 SWITCH	Press and hold REM pushbutton, then enter 07 and release REM pushbutton. Does the number displayed increment when the pushbutton and key switches are operated in the order given in tables 1 and 2?
Action		YES: Step 10 NO: Test M07 - Switch fault

STEP 10	08 REFERENCE BOARD TEST	Has a fault code appeared in the frequency display?
Action		NO: Step 11 YES: Test M08 - Reference generation fault.

NOTE: If the test sequence stops at this point when BITE testing without SCORE input, switch power off and on, and depress and release the REMOTE button prior to re-entering the required BITE number.

CAUTION: Avoid switching off with the unit in REMOTE mode, as it may lock up when next switched on. ALWAYS switch off in the LOCAL mode.

STEP 11	09 SYNTHESIZER BOARD TEST	Has a fault code appeared in the PILOT carrier display?
Action		NO: Step 12 YES: Test M09 - Synthesizer fault

STEP 12	10 MODULATION BOARD TEST (USB)	Has a fault code appeared in the PILOT carrier display?
Action		NO: Step 13 YES: Test M10 - USB fault

STEP 13	11 MODULATION BOARD TEST (LSB)	Has a fault code appeared in the PILOT carrier display?
Action		NO: Step 14 YES: Test M11 - LSB fault

STEP 14	12 MODULATION BOARD TEST (CARRIER)	Has a fault code appeared in the PILOT carrier display?
Action		NO: Step 15 YES: Test M12 - Carrier control or DAC fault.

STEP 15	13 MIXER BOARD TEST	Has a fault code appeared in the PILOT carrier display?
Action		NO: Step 16 YES: Test M13 - Mixer board fault

STEP 16

Connect a 50 ohm 0.25W dummy load to the RF OUTPUT connector on the rear panel. Press and release the ENTER pushbutton.

14
RF OUTPUT
BOARD TEST

Has a fault code appeared in the PILOT carrier display?

Action

NO: Step 17
YES: Test M14 - RF output board fault

STEP 17

Is the MA1723 fitted with the SCORE interface board?

Action

YES: Step 18
NO: Step 19

STEP 18

Connect the SCORE test plug (Chap. 19) to SK5 on the MA1723 rear panel. Press and release the ENTER pushbutton.

15
SCORE
INTERFACE
TEST

Is the FAULT legend iluminated?

Action

NO: Step 19
YES: Test M15 - SCORE interface fault

STEP 19

Press and hold the REM pushbutton, then enter 16 and release the REM pushbutton. Connect a 50 ohm 0.25W dummy load to the RF OUTPUT connector on the rear panel. Connect the oscilloscope (minimum bandwidth 5 MHz) to the RF monitor socket on the front panel. Press and release the ENTER pushbutton.

---

	16 KEYING TEST	Is the waveform displayed on the oscilloscope correct? (A carrier keyed at approximately 20 Hz).
Action		YES: Step 20 NO: Test M16 - CW keying fault

STEP 20		Press and hold the REM pushbutton, then enter 17 and release the REM pushbutton. Connect the amplifier test plug (Chap. 19) to SK6 on the rear panel. Press and release the ENTER pushbutton.
	17 AMPLIFIER CONTROL LINE TEST	Do the linear amplifier control and status LED indicators illuminate correctly when the appropriate pushbuttons are pressed?
Action		YES: Step 21 NO: Test M17 - Control line fault

STEP 21		Is the MA1723 fitted with the optional FSK board?
Action		YES: Step 22 NO: Press and release RCL (end of test).

STEP 22		Press and hold the REM pushbutton, then enter 19 and release the REM pushbutton. Connect a 50 ohm 0.25W dummy load to the RF OUTPUT connector on the rear panel. Connect the spectrum analyser or FSK receiver to the RF monitor socket on the front panel. Press and release the ENTER pushbutton.
	19 FSK KEYING TEST	Is FSK output correct? (An FSK signal keyed at 100 bauds (50 Hz) with a preset shift - see Chapter 19).
Action		YES: Press and release RCL (end of test) NO: Test M19 - FSK board fault

---

STEP 23	Has a fault code appeared in the frequency display?
Action	NO: Test M00/a YES: Test M00/b

SELF-TEST ROUTINE DESCRIPTION

Routine 00 - Power Supply Check (execution time 1 second)

5. This routine measures the levels of the +5V, +15V, -15V, +20V, +12V and -30V regulated supplies (in that order). If a supply is found to be outside the allowable voltage tolerance, the test sequence is stopped and the out-of-range supply is indicated on the frequency display. The display also indicates whether the faulty supply is above or below the allowable limit by displaying H for above or L for below. If a fault is found and the test sequence is resumed by pressing and releasing the ENTER pushbutton, the fault code legend will remain displayed until the end of test routine 03. If all of the supplies are within the specified limits, self-test routine 01 is automatically entered and executed.

Routine 01 - ROM Check Sum (execution time 7 seconds per ROM)

6. This routine performs a check sum calculation for each read only memory (ROM) device fitted to the processor board. Each byte stored in the ROM is transferred, in turn, to a register where its numeric value is added to that of the next byte, to arrive at a total figure for that particular ROM. This figure is then compared with the correct figure (stored in ROM), and if a difference is detected, the word FAULT, together with the circuit reference (PD number) of the faulty ROM device is indicated (in the frequency display). The test routine is then halted (by entering a continuous software loop). If, following the detection of a faulty ROM device, the test sequence is resumed by pressing and releasing the ENTER pushbutton, the fault display is maintained until the end of test 03. Whilst the ROM test is in progress, the ROM data is routed to the meter scale display. If the test sequence is completed successfully for each ROM device, self-test routine 02 is automatically entered and executed.

Routine 02 - RAM Test 1 (execution time 5 seconds)

7. This routine tests the RAM address lines for open and short circuits. Data is written to the meter display segments to indicate that the test is in operation. If an open or short circuit is detected, a mode legend will illuminate to indicate the faulty RAM address line, as follows, and FAULT is also illuminated.

MODE LEGEND	RAM ADDRESS LINE
PILOT (level)	7
FSK	6
CW	5
AM	4
PILOT	3
LSB	2
USB	1
ISB	0

8. If a RAM address line fault is detected, and the ENTER pushbutton is pressed and released to resume the test program, the fault display is maintained until the end of test 03. If the test is completed successfully, self-test routine 03 is entered and executed.

Routine 03 RAM Test 2 (execution time 5 seconds)

9. This routine tests the RAM data lines for open and short circuits. Data is written to the meter display segments to indicate that the test is in operation. If an open or short circuit is detected, a mode legend will illuminate to indicate the faulty data line, as follows, and FAULT is also illuminated.

MODE LEGEND	RAM DATA LINE
PILOT (level)	7
FSK	6
CW	5
AM	4
PILOT	3
LSB	2
USB	1
ISB	0

10. If a RAM data line fault is detected, and the ENTER pushbutton is pressed and released to resume the test program, the fault display is cleared immediately. If the test is completed successfully, self-test routine 04 is automatically entered and executed.

Routine 04 - EAROM Test (execution time 1 second)

11. This routine checks that data can be stored into and read back from one 4-bit location in each of the two EAROM devices on the processor board. A 'walking - 1' test pattern is used, as below. If the correct pattern is not read back then the appropriate mode legend is illuminated.

TEST PATTERN				ASSOCIATED MODE LEGEND
3	2	1	0	
0	0	0	1	ISB
0	0	1	0	USB
0	1	0	0	LSB
1	0	0	0	PILOT

12. The same test is carried out for each EAROM device. Since the EAROM at read address range 6000-63FF (ML2) is used to store channels 00 to 49, whilst the remaining EAROM (ML3 at read address range 7000 to 73FF) is used to store channels 50 to 99 plus the current front panel setting data, should a failure occur it is a simple matter to determine the faulty device.

13. If self-test routine 04 is completed successfully routine 05 is entered and executed.

Routine 05 - PIO Test (execution time 1 second)

14. This routine checks that a test pattern can be written into, and then read back from the PIO device (ML9) on the processor board. If the test fails, the FAULT indicator, together with a meter segment, are illuminated, and a numeral may appear in the frequency display. If the test routine is completed successfully, then self-test routine 06 is automatically entered and executed.

Routine 06 - Front Panel Display Test

15. This routine writes to all the display segments and the six LED indicators simultaneously for periods of four seconds on and four seconds off. The channel number display alternates between 04 and either 88 when the remaining display segments are on and blank when the remaining display segments are off. The cycle is repeated continuously, until either a new test routine is called or the RCL button is pressed and released. Note that one or more non-illuminated segments may be due to incorrect data from the processor rather than a faulty display device.

16. To continue with the self-test routine, press and hold the REM pushbutton, enter 07 and then release the REM pushbutton.

Routine 07 - Front Panel Switch Test

17. This routine checks for the correct action of the front panel switches. When the routine is entered, 01 appears in the frequency display, and this number increments after the correct action of the appropriate switch, as given in the following tables. When the last switch is operated (34 displayed), test routine 08 is automatically entered and executed.

Table 1: Pushbutton Switch Tests

INDICATED NUMBER	PUSHBUTTON TO BE PRESSED	INDICATED NUMBER	PUSHBUTTON TO BE PRESSED
01	REM	15	8
02	STD BY	16	9
03	EHT	17	STORE
04	TUNE	18	O/METER
05	MUTE	19	ENTER
06	RESET	20	FREQ
07	LOW POWER	21	CHAN
08	1/ISB1	22	RCL
09	2/ISB2	23	USB
10	3/ISB3	24	LSB
11	4	25	PILOT
12	5	26	AM
13	6	27	CW
14	7	28	FSK

Table 2: Lever Switch Tests

INDICATED NUMBER	LINE/SET/RF SWITCH POSITION	TX/PTT/VOX SWITCH POSITION
29	LINE	TX
30	SET	TX
31	RF	TX
32	RF	VOX
33	RF	PTT
34	RF	TX

Routine 08 - Reference Board Test (execution time 1 second)

18. This routine checks the following:

(a) 1.4MHz RF output level applied to the modulation board.
(b) 20MHz oscillator varactor voltage
(c) 40MHz RF output level to the mixer board

19. If a fault is detected, a fault code number in the range 1 to 6 is indicated in the frequency display and FAULT is also illuminated. The coding is as follows:

FAULT CODE	FAULT
1	1.4MHz RF output level low
2	1.4MHz RF output level high
3	20MHz oscillator varactor voltage low
4	20MHz oscillator varactor voltage high
5	40MHz RF output level low
6	40MHz RF output level high

20. If the test routine is completed successfully, test routine 09 is automatically entered and executed.

Routine 09 - Synthesizer Board Test (execution time 10 seconds)

21. Test routine 09 checks the following:

(a) that the varactor line voltage is within the allowable limits for synthesizer output frequencies of 41.4 MHz and 71.4 MHz.

(b) that the varactor line voltage level increases monotonically as the output frequency is increased from 41.4 MHz to 71.4 MHz in 1 MHz steps.

(c) that the varactor line voltage level increases monotonically as the output frequency is increased from 56.4 MHz to 57.39 MHz in 10KHz steps.

(d) that the RF output level remains within the allowable limits over the frequency range 42.4 MHz to 71.4 MHz in 1 MHz steps.

22. If a fault is detected, the word FAULT is displayed, the frequency at which the fault occurred is displayed, and a code number is indicated in the pilot carrier level display which relates to the following table:

FAULT CODE	FAULT
1	Varactor voltage low at 0 MHz
2	Varactor voltage high at 0 MHz
3	Varactor voltage low at 30 MHz
4	Varactor voltage high at 30 MHz
5	1 MHz steps, varactor voltage not monotonic
6	10 KHz steps, varactor voltage not monotonic
7	RF output level low
8	RF output level high

23. If the self-test routine is completed successfully, test routine 10 is automatically entered and executed.

Routine 10 - Modulation Board USB (execution time 20 seconds)

24. This self-test routine selects the USB Signal Path and switches off the LSB and carrier outputs. Initially, AGC is switched off and the residual RF output level is measured with no audio input. A test signal is then injected into the line 1 input amplifier (ML3a) and the d.c. level at TP3, the board RF output level and the d.c. level at TP11 are measured. The board RF output level is then measured, firstly with -2dB audio attenuation selected, and then with -6dB audio attenuation selected. Following this the mute signal is applied and the residual RF output level is measured. These tests are then repeated with AGC switched on. Finally, operation of the VOX circuit is tested.

FAULT CODE		TEST TONE	FAULT
AGC ON	AGC OFF		
00	14	OFF	Residual RF output level too high
01	15	-	Not used
02	16	ON	TP3 voltage level too high
03	17	ON	TP3 voltage level too low
04	18	ON	Board RF output level too high
05	19	ON	Board RF output level too low
06	20	ON	TP11 voltage level too high
07	21	ON	TP11 voltage level too low
08	22	ON	-2dB RF output level too high
09	23	ON	-2dB RF output level too low
10	24	ON	-6dB RF output level too high
11	25	ON	-6dB RF output level too low
12	26	ON	With audio muted RF output too high
13	27	-	Not used
28		ON	VOX not operational

25. If the self-test routine is completed successfully, routine 11 is automatically entered and executed.

Routine 11 - Modulation Board LSB (execution time 20 seconds)

26. This self-test routine repeats routine 10 (para. 24) for the LSB signal path, using the line 2 audio input amplifier (ML6a).

FAULT CODE		TEST TONE	FAULT
AGC ON	AGC OFF		
00	14	OFF	Residual RF output level too high
01	15	-	Not used
02	16	ON	TP4 voltage level too high
03	17	ON	TP4 voltage level too low
04	18	ON	Board RF output level too high
05	19	ON	Board RF output level too low
06	20	ON	TP13 voltage level too high
07	21	ON	TP13 voltage level too low
08	22	ON	-2dB RF output level is too high
09	23	ON	-2dB RF output level is too low
10	24	ON	-6dB RF output level is too high
11	25	ON	-6dB RF output level is too low
12	26	ON	With audio muted, RF output too high
13	27	-	Not used

27. If the self-test routine is completed successfully, routine 12 is automatically entered and executed.

Routine 12 - Modulation Board Carrier (execution time 5 seconds)

28. This self-test routine checks the carrier level control circuitry on the modulation board, as follows:

(a) that the OdBm carrier level is within the allowable limits

(b) that the -15dB carrier level is within the allowable limits

(c) that the board RF output level decreases monotonically when the carrier level is reduced in 1dB steps from OdBm to -30 dBm.

29. Should the modulation board fail any of these tests, then a fault code is indicated in the pilot carrier level display, as follows:

FAULT CODE	FAULT
OH	OdBm Carrier level too high
OL	OdBm Carrier level too low
1H	-15dBm Carrier level too high
1L	-15dBm Carrier level too low
02	Carrier not decreasing monotonically

30. If the self-test routine is completed successfully, routine 13 is automatically entered and executed.

Routine 13 - Mixer Board Test (execution time 10 seconds)

31. This routine measures the RF output level from the mixer board whilst the synthesized local oscillator signal is varied to sweep the RF output from 1 MHz to 30 MHz in 1 MHz steps, and the carrier level circuitry is set for a 0 dBm level carrier output from the modulation board. If a fault is detected, the frequency at which the failure occurred is displayed, and a fault code is indicated using the pilot carier level display, as follows:

FAULT CODE	FAULT
H	Mixer RF output level too high
L	Mixer RF output level too low

32. If the self-test routine is completed successfully routine 14 is automatically entered.

Routine 14 - RF Output Board Test (execution time 10 seconds)

33. When routine 14 is entered, either automatically from routine 13 or manually, the test number flashes on and off continuously to denote that operator intervention is required, i.e. a 0.25 watt 50 ohm dummy load must be connected to the RF outout socket on the rear panel to correctly load the RF output board. When this has been achieved, the ENTER pushbutton is pressed and released to terminate STANDBY on and EHT ON (if selected) and to start the test routine. This measures the RF output level from the unit with an output frequency of 15 MHz, and the carrier level control circuitry set for a 0 dBm carrier level from the modulation board. The measured RF output level is then used as a reference level as the drive unit output signal is swept from 1 MHz to 30 MHz in 1 MHz steps.

If the RF output level varies by more than the allowed amount, the frequency at which the test failed is displayed, and a fault code is indicated in the pilot carrier level display, as follows:

FAULT CODE	FAULT
H	RF output level too high
L	RF output level too low

34. If the test routine is completed successfully, routine 15 is automatically entered.

Routine 15 - Score Interface Test (SCORE versions only)

35. When routine 15 is entered, either automatically from routine 14 or manually, the test number flashes continuously to denote that the SCORE test plug (Chap. 19) must be connected to SK5 on the rear panel. The ENTER pushbutton is then pressed and released to start the routine. This tests the input and output user function lines, the start-in-sync (SIS) and master reset control lines, and the SCORE transmit and receive circuits. If a fault is detected, a fault code is indicated in the pilot carrier level display, as follows:

FAULT CODE	FAULT
1	User function line faulty
2	No sync. code or data after sync code received
3	Master reset not working
4	Corrupt data received or transmitted

36. If the self-test routine is completed successfully, routine 16 is automatically entered.

Routine 16 - CW Keying Test

37. When routine 16 is entered, either automatically from routine 15 or manually, the test number flashes continuously to denote that a 0.25 watt 50 ohm dummy load must be connected to the RF output socket on the rear panel, and an oscilloscope must be connected to the RF monitor socket on the front panel. The ENTER pushbutton is then pressed and released to start the routine, which initially ensures that STANDBY ON and EHT ON are de-selected. The routine then applies a 20 Hz keying waveform to the modulation board, sets the carrier control circuitry for a 0 dBm carrier level output from the modulation board, and sets the synthesizer for a drive unit output frequency of 5 MHz. The keying waveform simulates a string of morse code dots at a speed of 24 words per minute (120 characters per minute), which should be displayed on the oscilloscope.

38. This self-test routine runs continuously until cancelled by the selection of a different routine or until the RCL pushbutton is pressed and released.

Routine 17 - Linear Amplifier Control Test

WARNING SK6 on the MA1723 rear panel must NOT be connected to a linear amplifier for the duration of this test routine.

39. When this test is entered from the front panel, the test number flashes continuously to denote that the amplifier test plug (Chap. 19) must be connected to SK6 on the rear panel. The ENTER pushbutton is then pressed and released to start the routine. Press and release, in any order, the STANDBY, EHT, TUNE, MUTE, RESET and LOW POWER pushbuttons and check that the associated LED indicators illuminate. Press and release the same pushbuttons again and check that the associated LED indicators are extinguished.

40. This self-test routine runs continuously until cancelled by the selection of a different routine, or until the RCL pushbutton is pressed and released.

Routine 18 - DAC and I/O Strobe Test

41. When this routine is entered from the front panel, the test number flashes continuously so that the oscilloscope may be connected to TP26 on the front panel interface board to monitor the DAC (digital-to-analogue converter) output test signal, or to test points 13 to 21, 23, 24 or 25 (also on the front panel interface board) to monitor the I/O strobe lines. When the ENTER pushbutton is pressed and released, the routine causes the DAC output to continuously ramp from 0V to +10V with a saw tooth waveshape, and it causes a positive-going strobe pulse to appear on each I/O strobe line. This self-test routine runs continuously until cancelled by the selection of a different routine or until the RCL pushbutton is pressed and released.

Routine 19 - FSK Keying Test (FSK versions only)

Before selecting this routine, exit from the self-test mode (press RCL) and select a mode other than FSK.

42. When this test routine is entered from the front panel, the test number flashes continuously to indicate that a 0.25 watt 50 ohm dummy load must be connected to the RF output socket, and a spectrum analyser must be connected to the RF monitor socket on the front panel. When the ENTER pushbutton is pressed and released, the test number stops flashing, the STANDBY and EHT ON conditions are removed (if selected), the synthesizer is set to produce a drive unit output frequency of 5 MHz, and the modulation board is set for USB with FSK selected. A 50 Hz keying waveform is then applied to the FSK board, and the resulting output signal may be viewed on a spectrum analyser or monitored on an FSK receiver. This test routine runs continuously until cancelled by the selection of a different test or until the RCL pushbutton is pressed and released.

NOTE: If the unit is not equipped with the optional FSK board and test routine 19 is selected, the test number flashes continuously and operation of the ENTER pushbutton has no effect.

Routine 20 FSK Tone Test

Before selecting this routine, exit from the self-test mode (press RCL) and select a mode other than FSK.

43. When this routine is entered from the front panel, the test number flashes continuously to indicate that a 0.25 watt 50 ohm dummy load must be connected to the RF output socket on the rear panel, and that a frequency counter must be connected to the RF monitor socket on the front panel. When the ENTER pushbutton is pressed and released, the test number stops flashing, the STANDBY and EHT ON conditions are removed (if selected), the synthesizer is set to produce a drive unit output frequency of 5 MHz, and the modulation board is set to USB with FSK selected. Either of the two FSK tones may now be selected by pressing and releasing the FSK mode pushbutton. If the FSK board is set up for normal keying, the FSK mode legend illuminates to indicate that the higher frequency (MARK) tone has been enabled. A further press and release of the FSK mode pushbutton then enables the lower frequency (SPACE) tone, and the FSK mode legend is extinguished. The frequency of each tone is found by subtracting 5 MHz from the indicated frequency on the frequency counter. This test routine runs continuously until cancelled by the selection of a different test or until the RCL pushbutton is pressed and released.

NOTE: If the unit is not equipped with the optinal FSK board and self-test routine 20 is selected, the test number flashes continuously and operation of the ENTER pushbutton has no effect.

Routine 21 - Synthesizer Signature Analysis Test

44. Test routine 21 is one of four programs which is used to set up the drive unit for signature analyser testing (the remaining three programs are selected using switches, on the processor board). Full details of the signature analysis technique are given in Chapter 20.

CHAPTER 19

FUNCTIONAL TEST AND ALIGNMENT

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Tables

Illustrations

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CHAPTER 19

FUNCTIONAL TEST AND ALIGNMENT

INTRODUCTION

1. This chapter contains a functional test procedure followed by the alignment procedure. The functional test procedure may be carried out as part of a routine maintenance schedule or as an aid to fault location.

TEST EQUIPMENT

2. The items of test equipment listed below are required for the following procedures:

(1) RF millivoltmeter
Input impedance: 50 ohms
(Example: Racal-Dana Instruments 9301A)

(2) Frequency Counter with an internal reference output
(Example: Racal-Dana Instruments 9912)

(3) Spectrum Analyser/Tracking Generator
(Example: Hewlett Packard 141T, 8552B, 8553B/8443B, or Marconi TF2370)

(4) Two-Tone Audio Signal Generator
(Example: Racal-Dana Instruments 9083)

(5) Digital Multimeter
(Example: Racal-Dana Instruments 4002)

(6) Oscilloscope, dual trace
(Example: Tektronix 465 or Hewlett Packard 1740A)

(7) Monitor Receiver
(Example: Racal RA1792)

(8) Telephone Handset, fitted with PO plug 420
(Example: Racal AA651/G)

(9) Step Attenuator
Range: 0 to 100 dB in 1 dB steps
Impedance: 50 ohms
(Example: Samwell and Hutton Type 129)

(10) 20 dB Attenuator, 50 ohms
(Example: Marconi TM5573)

(11) Test leads 1 and 2 - figs. 19(a) and 19(b) comprising:

*Plug 25-way (to mate with SK4)
*Plug 15-way (to mate with SK6)
Three-off 12-way terminal blocks
Nine-off 10K, 0.25W resistors (914042)
Single-pole 2-way switch (KEY switch)
Single-pole changeover switch (FSK versions only)
Connecting wire

(12) *Plug, 15-way (Amplifier test plug - fig- 19(c))

(13) 0.25 watt, 50 ohm BNC dummy load.

The remaining items only required when the MA1723 is fitted with the optional SCORE interface board.

(14) Serial Data Test Set Racal CA617

(15) Test lead 3 - fig. 19(h) - comprising:

*Plug, 25-way (to mate with CA617 - SK5)
*Plug, 37-way (to mate with MA1723 - SK5)
10-way terminal block

(16) *Plug, 37-way (SCORE test plug - fig. 19(g))

* For connector part numbers see Chap. 2.

FUNCTIONAL TEST

3. The following functional test procedures make use of the self-test routines described in Chapter 18. Any indicated faults must be rectified before continuing with the test procedures. The procedures should be carried out in the order given.

Preliminary

4. (1) Where applicable, disconnect all rear panel connectors, remove the unit from the rack or cabinet, and place it on a flat, clean working surface.

(2) Make up the two test cables, as shown in figs. 19(a) and 19(b). Connect test cable 1 to SK4 and test cable 2 to SK6.

(3) Make up the amplifier test plug as shown in fig. 19(c).

(4) Set the KEY switch connected to test cable 1 to the open position.

(5) Ensure that the orientation of the supply voltage selector card located beneath the supply fuse on the rear panel is correct for the intended source of supply.

(6) Set the front panel POWER switch to ON.

(7) Press and release the RESET pushbutton.

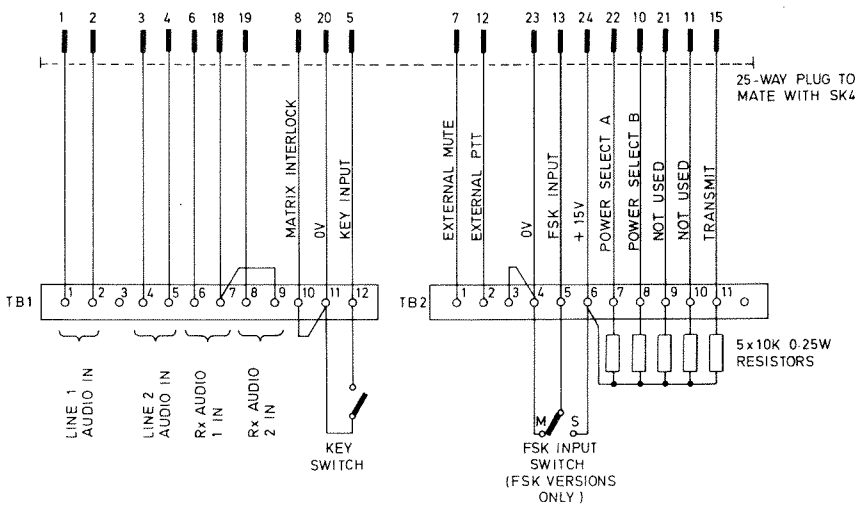


Fig. 19(a) Test Lead 1

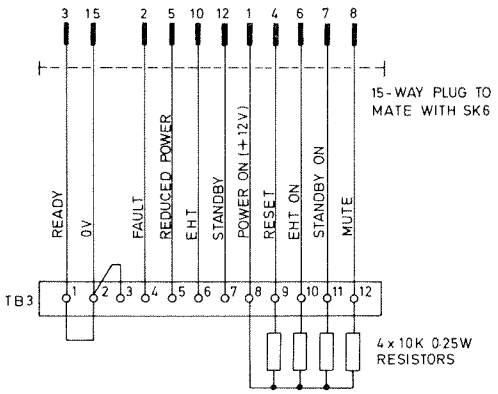


Fig. 19 (b) Test Lead 2

Fig. 19 (c) Amplifier Test Plug

Self-Test Routines

5. Carry out self-test routines 00 to 14, 16 and 17, as follows (para. 6) and check that no faults are indicated. Any indicated fault must be rectified before continuing. Note that a fault detected whilst carrying out tests 08 to 13 may be due to an incorrectly adjusted board or pub-assembly. Tabulated below is the corresponding realignment procedure paragraph, given elsewhere in this chapter. For an interpretation of the results of the self-test routines, refer to chapter 18.

Test No.	Paragraph
08	19 - Reference Generator Board
09	20 - Synthesizer Board
10	
11	26 - Modulation Board
12	
13	21 - Mixer Board

6. (1) To enter the self-test mode, press and hold the REM pushbutton, press and release the 0 pushbutton twice, and then release the REM pushbutton. Test number 00 appears in the left-hand display panel (channel number position), and tests 00 to 06 are executed automatically, in sequence.

(2) In test 06, the liquid crystal display segments and the six LED indicators are continually flashed on and off so that they may be checked for correct operation (compare with fig. 3.1, Chap. 3)

(3) To terminate test 06 and enter test 07, press and hold the REM pushbutton, press and release 0 followed by 7, and then release the REM pushbutton. Test number 07 should be displayed, and 01 should also be displayed on the left hand display panel (frequency position).

(4) Press and release the REM pushbutton and check that the frequency display changes from 01 to 02.

(5) Press and release the remaining front-panel pushbuttons, in sequence, as listed in table 1, and check that the appropriate numerals are displayed.

(6) When numeral 29 is displayed, set the LINE/SET/RF and VOX/PTT/TX switches to the positions given in table 2 and check that the correct numerals are displayed.

(7) On completion of test 07, tests 08 to 13 are executed automatically, and in sequence. After completion of test 13, test number 14 repeatedly flashes to indicate that operator intervention is required. Connect a 0.25 watt, 50 ohm BNC dummy load to the RF output socket on the rear panel, and then press and release the ENTER pushbutton to start the test.

(8) Test 15 is concerned with the optional SCORE interface board and is dealt with elsewhere in this chapter. When a flashing test number 15 is observed, press and hold the REM pushbutton, press and release 1 followed by 6, and then release the REM pushbutton.

(9) When selected, test number 16 flashes repeatedly to indicate that operator intervention is required. Connect the oscilloscope to the RF monitor connector on the front panel, ensure that a 0.25 watt 50 ohm dummy load is connected to the RF output socket on the rear panel, and then press and release the ENTER pushbutton to start the test. A 20 Hz keying waveform is applied to the modulation board which is set to produce a 0 dBm keyed carrier, and the synthesizer is set to produce a 5 MHz RF signal at the output of the drive unit. The waveform displayed on the oscilloscope should therefore simulate a string of Morse code dots being sent at a speed of 24 words per minute (120 characters per minute). To terminate this test, select test number 17.

(10) Test number 17 repeatedly flashes to indicate operator intervention. Connect the amplifier test plug shown in fig. 19(c) to SK6 on the rear panel, and then press and release the ENTER pushbutton to start the test. Press and release, in turn, the STANDBY, EHT, TUNE, MUTE, RESET and LOW POWER pushbuttons and ensure that the associated LED indicator illuminates. Press and release the pushbuttons again and ensure that the associated LED indicators are extinguished.

Table 1: Pushbutton Tests

INDICATED NUMBER	PUSHBUTTON TO BE PRESSED	INDICATED NUMBER	PUSHBUTTON TO BE PRESSED
01	REM	15	8
02	STD BY	16	9
03	EHT	17	STORE
04	TUNE	18	0/METER
05	MUTE	19	ENTER
06	RESET	20	FREQ
07	LOW POWER	21	CHAN
08	1/ISB1	22	RCL
09	2/ISB2	23	USB
10	3/ISB3	24	LSB
11	4	25	PILOT
12	5	26	AM
13	6	27	CW
14	7	28	FSK

Table 2: Lever Switch Tests

INDICATED NUMBER	LINE/SET/RF SWITCH POSITION	TX/PTT/VOX SWITCH POSITION
29	LINE	TX
30	SET	TX
31	RF	TX
32	RF	VOX
33	RF	PTT
34	RF	TX

(11) Press and release the RCL pushbutton to exit from the self-test routines.

NOTE To exit from the self-test mode, at any time, press and release the RCL pushbutton. A prior condition exists for test number 07 in that the number displayed at the frequency position must be 03 or higher before the exit can be achieved. If, during any self-test, the exit condition is not achieved by pressing and releasing the RCL pushbutton, set the unit POWER switch to OFF and then back to ON.

(12) Ensure that REMOTE is not selected (REMOTE not displayed in the left-hand display panel). If it is, press and release the REM pushbutton.

EAROM PROGRAMMING

7. (1) Load the channels given in table 3 with the stated frequency and mode data, as follows:

(2) Set the required frequency and mode.

(3) Press and hold the STORE pushbutton. The word CHANNEL is displayed (if not already displayed) and the previously displayed channel number is blanked.

(4) Use the numeric pushbuttons to select the required channel number, most significant digit first.

(5) Release the STORE pushbutton to store the receiver settings in the selected channel.

Table 3: EAROM Channels

CHANNEL	FREQUENCY (KHz)	MODE
01	01 000.0	USB
11	11 111.1	LSB
21	22 222.2	USB
31	23 333.3	LSB
41	24 444.4	USB, PILOT
51	25 555.5	LSB, PILOT
61	26 666.6	AM
71	27 777.7	CW
81	28 888.8	ISB1
91	29 999.9	ISB1

(6) Connect the test equipment as given in fig. 19(d).

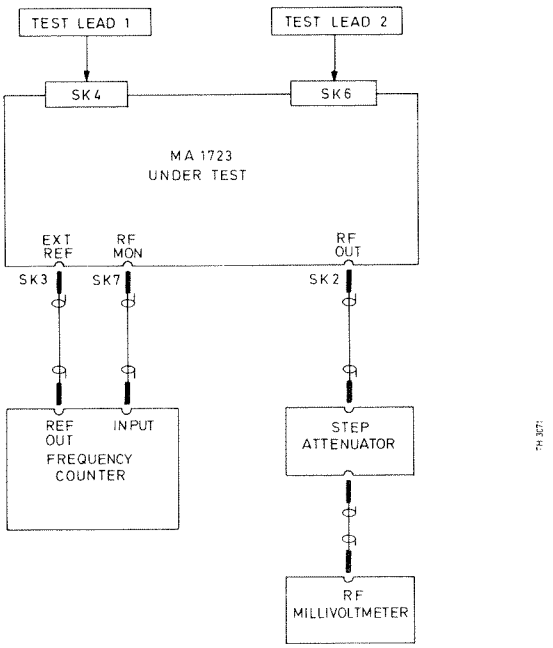


Fig. 19 (d) Test Equipment Connections 1

(7) Set the step attenuator to 13 dB.

(8) At the MA1723 set the frequency to 15 000.0 KHz, press and release the CW pushbutton, and set the VOX/PTT/TX switch to TX. Close the KEY switch connected to SK4 and adjust R1 on the RF output board for an RF millivoltmeter indication of +10 dBm. Open the KEY switch connected to SK4.

(9) Press and release the TUNE pushbutton.

(10) Select, in turn, the channels given in table 1 (press and release the CHAN pushbutton, use the numeric pushbuttons to select the required channel number, and then press and release the ENTER pushbutton), and then check that

(a) The CHANNEL, FREQUENCY and MODE displays are correct

(b) The frequency counter indication is within ±1Hz of the specified channel frequency

(c) The variation in RF output level from channel 01 to channel 91 does not exceed 2dB.

NOTE: The actual RF level indicated is dependent on the preset TUNE carrier level (see Chap. 2)

(d) Cancel the TUNE condition by pressing and releasing the TUNE pushbutton.

Internal Frequency Standard

8. If the unit is fitted with an internal frequency standard (type 9442 or 9420), carry out the following test.

(a) Disconnect the reference input from SK3 on the rear panel.

(b) Set the drive unit to a frequency of 10 000.0 kHz and select TUNE.

(c) Ensure that the frequency counter indicates 10 000 kHz ± 2 Hz. (This assumes a frequency counter standard better than 1 part in 10^7).

(d) Reconnect the reference input to SK3.

Output Levels

9. (1) Ensure that the test equipment is connected as shown in fig. 19(d), and that the step attenuator is set to 13 dB. Set AGC switches SA and SB on the modulation board to the ON position.

(2) At the MA1723, set the frequency to 15 000.0 kHz, select the CW mode and set the VOX/PTT/TX switch to TX.

(3) Close the KEY switch connected to SK4 and check that the RF millivoltmeter indicates +10 dBm ±1 dB. Note the level as a reference.

(4) Set the LINE/SET/RF meter switch to the RF position and check that the front panel metering display indicates +23dBm ±2dB.

(5) Open the KEY switch and select the AM mode. Ensure that the RF millivoltmeter indicates -6dB ±1dB relative to the reference level established at step (3).

(6) Select USB and PILOT. Check that USB, PILOT, and a pilot carrier level in the range -10dB to -30dB (as preset) are illuminated on the right hand display panel.

(7) Ensure that the RF millivoltmeter indication is within 1 dB of the reference level minus the displayed pilot carrier level, i.e. if a pilot carrier level of -20dB is displayed, ensure that the RF millivoltmeter indicates -20dB ±1dB relative to the reference level established at step (3).

(8) Connect the audio signal generator, set for single tone operation, to TB1 of test lead 1, pins 1 and 2 (line 1 audio input).

(9) Set the audio signal generator to a frequency of 1 kHz and an output level of 0dBm.

(10) At the MA1723, select LSB and set the LINE/SET/RF output to LINE.

(11) Ensure that LINE 1 is indicated on the right-hand display panel and that the audio meter display indicates 0dBm ±1dB.

(12) Set the LINE/SET/RF switch to the SET position, and check that SET 1 and the audio meter scale are illuminated on the right-hand display panel.

(13) If necessary, adjust the LINE 1 control on the rear panel for a front panel meter indication of 0dBm.

(14) Ensure the level indicated on the RF millivoltmeter is within ±1dB of the reference level established at step (3). Note the level.

(15) Increase the audio signal generator output level to +10dBm and ensure that the RF millivoltmeter indication is within ±1dB of the level noted at step (14).

(16) Reduce the audio signal generator output level to -10dBm and ensure that, after settling, the RF millivoltmeter indication is within ±1dB of the level noted at step (14).

(17) Set the audio signal generator output level to 0dBm.

(18) At the MA1723 select USB and ensure that the front panel meter indicates 0dBm ±1dB and that the RF millivoltmeter indication is within ±1dB of the reference level established at step (3). Note the level.

(19) Increase the audio signal generator output level to +10dBm and ensure that the RF millivoltmeter indication is within ±1dB of the level noted at step (18).

(20) Reduce the audio signal generator output level to -10dBm and ensure that the RF millivoltmeter indication is within ±1dB of the level noted at step (18).

(21) Set the audio signal generator output level to 0dBm.

(22) Select ISB1 and check that the RF millivoltmeter indicates -6dB ±1dB relative to the level noted at step (18).

(23) Transfer the audio signal generator to pins 3 and 4 of TB1 (line 2 audio input).

(24) At the MA1723 set the LINE/SET/RF switch to the LINE position, and press and release the METER pushbutton. Check that LINE 2 is indicated on the right-hand display panel and that the audio meter display indicates 0dBm ±1dB.

(25) Set the LINE/SET/RF switch to the SET position and press and release the METER pushbutton. Check that SET 2 is indicated on the right-hand display panel.

(26) If necessary, adjust the LINE 2 control on the rear panel for an indicator of 0dBm on the front panel meter. Ensure that the RF millivoltmeter indication is -6dB ±1dB relative to the level noted at step (14). Disconnect the audio signal generator.

(27) At the MA1723 select the CW mode and check that the VOX/PTT/TX switch is set to TX.

(28) Close the KEY switch connected to TB1 (of test lead 1) and ensure that the RF millivoltmeter indication is within ±1dB of the reference level established at step (3). Open the KEY switch.

(29) Connect the multimeter, set to the 25V d.c. range, positive lead to TB3 pin 12 (MUTE) and the negative lead to TB5 pin 5 (0V) of test lead 2. Ensure that the multimeter indicates approximately +12 V.

(30) Set the VOX/PTT/TX switch to VOX. Close the KEY switch and ensure that the RF millivoltmeter indication is within ±1dB of the reference level established at step (3).

(31) Check that the multimeter indicates approximately +12V. Open the KEY switch, check that the RF output drops immediately, and that the multimeter indication falls to approximately 0V after approximately one second. Disconnect the multimeter.

Amplifier Control

10. (1) Ensure that the test equipment is connected as shown in fig. 19(d), and that the step attenuator is set to 13dB.

(2) Connect a temporary wire link between TB3 pin 5 (REDUCED POWER) and TB3 (0V) on test lead 2.

(3) At the MA1723, set the VOX/PTT/TX switch to PTT.

(4) Ensure that TB3 pin 1 (READY) is linked to TB3 pin 2 (OV) on test lead 2.

(5) At the MA1723 set the POWER switch to OFF and then back to ON; ensure that the RESET LED is illuminated, and that the remaining LED indicators are extinguished.

(6) Use the multimeter, set to the 25V d.c. range, to monitor the levels at pins 9, 10, 11 and 12 of TB3 (multimeter negative lead connected to TB3 pin 3), and ensure they are as follows:

TB3/9	RESET	OV
TB3/10	EHT ON	+12V
TB3/11	STANDBY ON	+12V
TB3/12	MUTE	OV

(7) At the MA1723, press and release the RESET pushbutton. Ensure that at the MA1723 the RESET LED is extinguished, and that READY is indicated in the right-hand display panel.

(8) Using the multimeter, check that the voltage level at TB3 pin 12 (MUTE) has risen to approximately +12V.

(9) Connect a temporary wire link between TB3 pin 7 (STANDBY) and TB3 pin 3 (OV). Ensure that the front panel STANDBY LED illuminates. Remove the temporary link and ensure that the STANDBY LED is extinguished.

(10) Connect a temporary wire link between TB3 pin 6 (EHT) and TB3 pin 3 (OV). Ensure that the front panel EHT LED illuminates. Remove the temporary link and ensure that the EHT LED is extinguished.

(11) Press and release the STANDBY pushbutton. Using the multimeter, check that the voltage level at TB3 pin 11 (STANDBY ON) has fallen to approximately 0 V.

(12) Press and release the EHT pushbutton. Using the multimeter, check that the voltage level at TB3 pin 10 (EHT ON) has fallen to approximately 0 V.

(13) Press and release the STANDBY pushbutton. Using the multimeter, check that the voltage levels at TB3 pins 10 and 11 have both risen to approximately +12 V.

(14) Remove the temporary wire links from TB3 pins 3 and 5.

(15) Check that RED PWR is indicated on the right-hand display panel.

Intermodulation Products and In-Band Noise

11. (1) Connect the test equipment as shown in fig. 19(e).

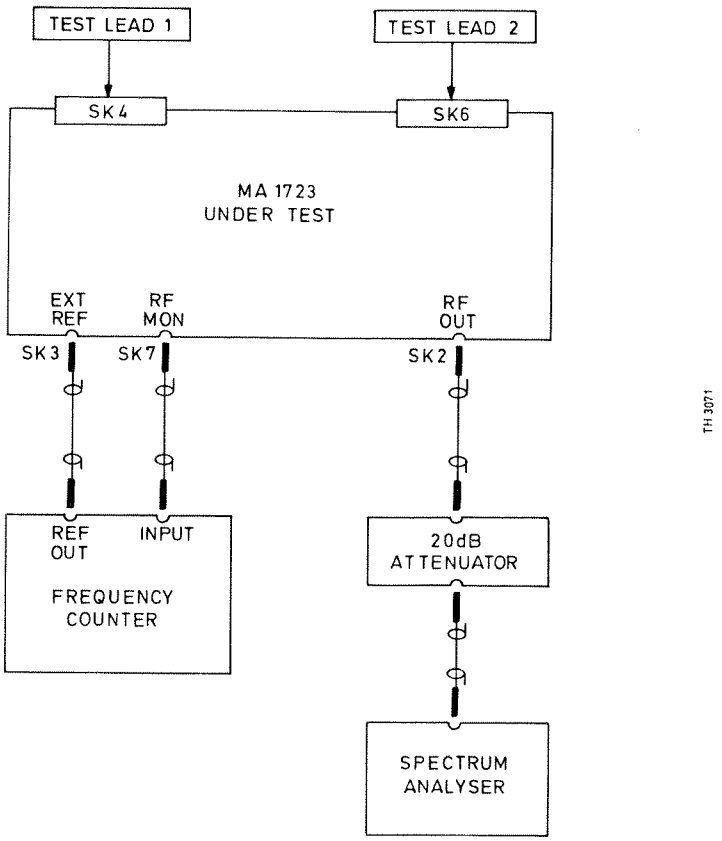


Fig. 19 (e) Test Equipment Connections 2

(2) Ensure that TB1 pin 10 (MATRIX INTERLOCK) is connected to TB1 pin 11 (OV), and that TB3 pin 1 (READY) is connected to TB3 pin 2 (OV), on test leads 1 and 2 respectively.

(3) Connect the audio signal generator to terminals 1 and 2 of TB1 (LINE 1 AUDIO IN).

(4) Set the audio signal generator for single tone operation at 1KHz, output level 0dBm.

(5) At the MA1723, set the frequency to 15 000.0 kHz, MODE to USB, and set the VOX/PTT/TX switch to TX.

(6) Set the spectrum analyser as follows:

Centre frequency:	15 000.0 kHz
Horizontal scale:	1 kHz/div
Vertical scale:	10 dB/div
Bandwidth:	30 Hz

(7) Adjust the spectrum analyser to display the USB signal at the top of the screen. Ensure that the in-band noise and sidebands are not less than 50 dB below the top of the screen.

(8) Repeat step (7) with the MA1723 and the spectrum analyser set to frequencies of 01 000.0 kHz and 29.999.9 kHz.

(9) Set the audio signal generator for two-tone operation at 1.0 kHz and 1.7 kHz. Set the level of each tone to -10dBm.

(10) Set the MA1723 to 15 000.0 kHz, USB. Adjust the spectrum analyser to display the two-tone signal at the top of the screen and ensure that the third order intermodulation products are not less than 50dB below either tone.

(11) Select LSB and ensure that the third order intermodulation products are not less than 50dB below either tone.

(12) Set the MA1723 and the spectrum analyser to 01 000.0 kHz. Adjust the spectrum analyser to display the two-tone signal at the top of the screen and ensure that the third order intermodulation products are not less than 50dB below the top of the screen.

(13) Repeat step (12) with the MA1723 and the spectrum analyser set to 29.999.9 kHz.

Muting

12. (1) Connect the test equipment as shown in fig. 19(e).

(2) Ensure that TB1 pin 10 (MATRIX INTERLOCK) is connected to TB1 pin 11 (0V) and that TB3 pin 1 (READY) is connected to TB3 pin 2 (0V), on test leads 1 and 2 respectively.

(3) Set the MA1723 to a frequency of 29.999.9 kHz, MODE to CW. Set the VOX/PTT/TX switch to TX.

(4) Set the spectrum analyser as follows:

Centre frequency:	29 999.9 kHz
Horizontal scale:	1kHz/div.
Vertical scale:	10dB/div.
Bandwidth:	100Hz

(5) Close the KEY switch (connected to test lead 1) and adjust the spectrum analyser to display the CW signal at the top of the screen.

(6) Open the KEY switch and ensure that the CW signal decreases by not less than 55dB.

(7) Close the KEY switch. Press and release the front panel MUTE pushbutton and ensure that the CW signal decreases by not less than 70dB.

(8) Open the KEY switch.

Microphone and PTT Operation

13. (1) Connect the test equipment as shown in fig. 19(f).

(2) Ensure that TB1 pin 10 (MATRIX INTERLOCK) is connected to TB1 pin 11 (OV), and that TB3 pin 1 (READY) is connected to TB3 pin 2 (OV), on test leads 1 and 2 respectively.

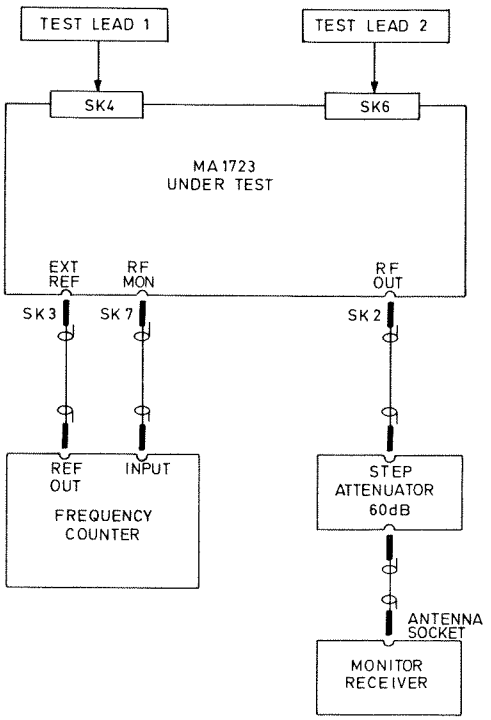


Fig.19 (f) Test Equipment Connections 3

(3) At the MA1723, set the frequency to 15 000.0 kHz, MODE to USB. Set the VOX/PTT/TX switch to PTT.

(4) Connect the telephone handset to the LINE 1 socket on the front panel.

(5) Press the PTT switch on the telephone handset and using the microphone voice modulate the MA1723 output signal. Monitor the transmission using the monitor receiver and ensure that it is clear and undistorted. Ensure that audio sidetone is present in the handset earpiece.

(6) Repeat step (5) with the MA1723 set, in turn, to USB + PILOT, LSB, AM and ISB1.

(7) Set the VOX/PTT/TX switch to VOX.

(8) Using the microphone ensure that the VOX circuit operates. Monitor the transmission using the monitor receiver and ensure that it is clear and undistorted.

(9) At the MA1723, select ISB1 and transfer the telephone handset to the LINE 2 socket. Set the VOX/PTT/TX switch to PTT.

(10) Press the PTT switch on the telephone handset, and using the microphone, voice modulate the MA1723 output signal. Monitor the transmission using the monitor receiver and ensure that it is clear and undistorted. Ensure that audio sidetone is present in the handset earpiece.

(11) Set the MA1723 to the CW mode and set the VOX/PTT/TX switch to TX. Transfer the telephone handset to the LINE 1 socket.

(12) Close the KEY switch (connected to test lead 1) and ensure that the audio sidetone oscillator signal is present in the telephone handset earpiece.

(13) Open the KEY switch.

FSK Test (FSK versions only)

14. (1) Connect the test equipment as shown in fig. 19(d). Set the step attenuator to -13dB.

(2) Ensure that TB1 pin 10 (MATRIX INTERLOCK) is connected to TB1 pin 11 (OV, and that TB3 pin 1 (READY) is connected to TB3 pin 2 (OV), on test leads 1 and 2 respectively.

(3) At the MA1723, set the frequency to 15 000.0 kHz and select TUNE. Ensure that the RF millivoltmeter indicates +10dBm ±1dB. Note the level.

(4) Cancel TUNE and select FSK.

(5) Set the VOX/PTT/TX switch to TX.

(6) Set the FSK INPUT switch (connected to test lead 1) to the mark (M) position, and check that the frequency counter indicates 15 000.000 kHz plus or minus the preset shift frequency (in the range 42Hz to 425Hz). Note the shift frequency, i.e. add or subtract, as appropriate, 15 000.000 kHz from the displayed frequency, and record the difference.

(7) Ensure that the RF millivoltmeter indication is within ±1dB of that noted at step (3).

(8) Set the FSK INPUT switch to the space (S) position and check that the deviation from 15 000.000 kHz is within ±5% of the shift frequency recorded at step (2).

NOTE

1. When the unit leaves the factory, the frequency shift is set to plus and minus 400Hz. For the adjustment procedure, see para 35.

2. The direction of the frequency shift for a particular setting of the FSK INPUT switch is also dependent on the positioning of links LK1 and LK2 on the FSK board.

3. Self-test routines 19 and 20 may be used to test the FSK board - see Chap. 18.

SCORE Interface Tests (SCORE version only)

15. (1) Disconnect all test leads and test equipment from the MA1723.

(2) Connect the SCORE test plug shown in fig. 19(g) to SK5 on the MA1723 rear panel.

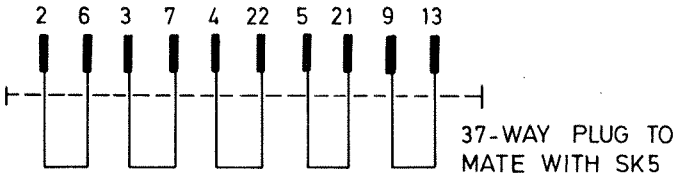


Fig. 19 (g) Score Test Plug

(3) Press and hold the REM pushbutton, press and release 1 followed by 5, and then release the REM pushbutton.

(4) Check that a flashing test number 15 is displayed and then press and release the ENTER pushbutton to start the test.

(5) If the test is successfully completed, a flashing test number 16 is displayed almost immediately following the press and release of the ENTER button. If the test is not successful, a fault code is displayed and reference should be made to Chap. 18 for further information.

(6) Press and release the RCL pushbutton to exit from the self-test routine.

(7) Remove the SCORE test plug from SK5 on the rear panel, reconnect test lead 1 to SK4 and reconnect test lead 2 to SK6.

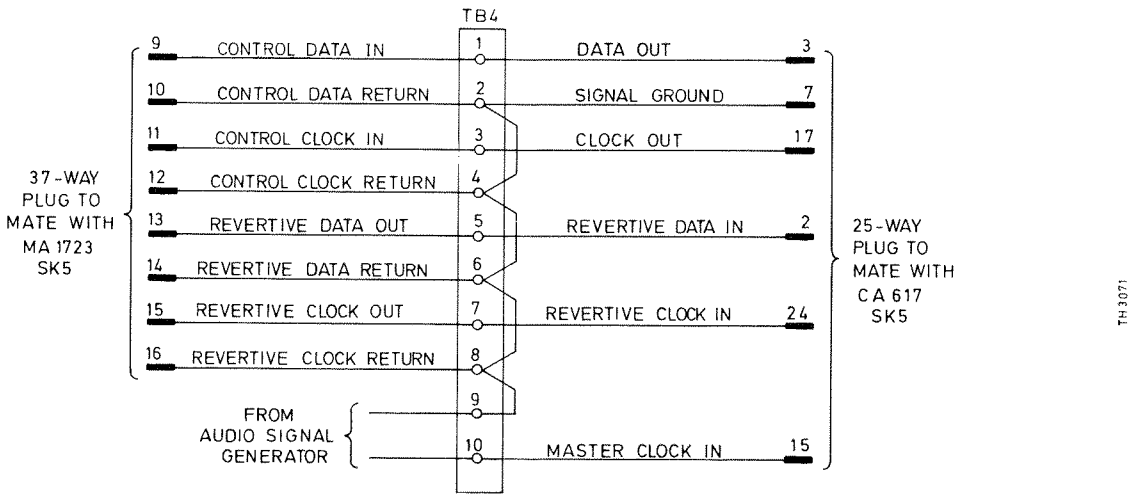


Fig.19(h) Test Lead 3 (SCORE)

(8) Connect the 37-way plug of test lead 3 to SK5 on the MA1723 rear panel.

(9) Connect the 25-way plug of test lead 3 to SK5 on the CA617 rear panel.

(10) Connect the audio signal generator, set for single tone operation and to a frequency of approximately 4800Hz, to TB4 of test lead 3, pins 9 (earth) and 10.

(11) Set the audio signal generator output level to approximately 5V.

NOTE: The CA617 internally generated clock signal runs at 19.2 kHz. Since this is too high for satisfactory operation of the MA1723, an externally procuded master clock signal must be provided for application to the CA617. This external clock signal (in this case the 4800Hz output from the audio signal generator) automatically overrides the internally generated clock signal.

(12) Set the switches on the CA617 as follows:

SINGLE FRAMES	UP (off)
ADDRESS WORD SEND	UP (off)
Remaining ADDRESS WORD switches	Not Applicable
RETURN MONITOR	UP (off)
CONTROL INHIBIT	UP (off)
TRANSMIT	UP (off)
SUPPLY	ON

(13) Set the FORWARD DATA switches for words X and Y as follows:

X	2	9	8	7	6	5	0	0	1
	8	7	6	5	4	3	2	1	WORD
Y	0	0	3	6	0	A	0	0	3
	8	7	6	5	4	3	2	1	WORD

(14) Set the FORWARD DATA X and Y SEND switches to on. Check that READY is indicated on the front panel display. If not, press and release the RESET pushbutton.

(15) Set the MA1723 to REMOTE and ensure that the front panel displays are as follows:

FREQUENCY	29876.5 kHz
MODE	USB
PILOT LEVEL	-26dB
TUNE LED	ON
STANDBY LED	OFF
EHT LED	OFF
MUTE LED	OFF
RESET LED	OFF
LOW POWER LED	OFF

(16) At the CA617 set the REVERTIVE DATA WORD switch to 1.

(17) Check that the REVERTIVE DATA display is as follows:

2	9	8	7	6	5	0	0	0
8	7	6	5	4	3	2	1	0

(18) Set the REVERTIVE DATA WORD switch to 3 and check that the REVERTIVE DATA display is as follows:

8	0	3	6	0	A	0	0	0
8	7	6	5	4	3	2	1	0

(19) Set the REVERTIVE DATA WORD switch to 0 and check that the REVERTIVE DATA display is as follows:

0	0	0	1	8	8	0	0	0
8	7	6	5	4	3	2	1	0

(20) Switch off and disconnect all test equipment.

ALIGNMENT PROCEDURES

16. Under normal operating conditions the drive unit will maintain the factory alignment over a long period of time. Re-alignment should therefore, only be carried out following the replacement of an assembly or components which affect the alignment, or where a known mis-alignment exists.

17. Should it be necessary to re-align the complete drive unit, the following procedures should be carried out in the order given. Before attempting to re-align an individual assembly, it must be ascertained, where applicable, that the preceding assemblies are functioning correctly. If the specified performance cannot be attained by re-alignment, then a fault must be suspected and reference should be made to Chapter 20.

18. A limited amount of dismantling is necessary to gain access to certain areas of the drive unit. After alignment, ensure that all screening covers are replaced.

REFERENCE GENERATOR BOARD

19. (1) Position the unit underside up on the working surface. Remove (if fitted) the overall cover plate and the cover from the reference generator board compartment.

(2) Connect the 1MHz reference output signal from the frequency counter to SK3 on the rear panel of the MA1723. Set the frequency counter to operate from its internal standard.

(3) Remove the coaxial socket from PL30 on the reference generator board, and connect PL30 via the 20dB attenuator to the frequency counter. Ensure that the frequency counter indicates 20 000 000 Hz plus or minus 1Hz. Disconnect the 20dB attenuator and the frequency counter input.

(4) Connect the RF millivoltmeter to PL30 on the reference generator board. Ensure that it indicates 0dBm plus or minus 3dB. Disconnect the RF millivoltmeter and replace the coaxial socket removed from PL30.

(5) Remove the coaxial socket from PL29 on the reference generator board, and connect PL29 to the RF millivoltmeter. Repeatedly adjust transformers T3 and T4 for a maximum indiction on the RF millivoltmeter. Ensure that the RF millivoltmeter indicates 0dBm plus or minus 3dB.

(6) Connect the digital multimeter between ML10 pin 6 and chassis, and check that it indicates between 6.0 and 12.0 volts d.c. disconnect the digital multimeter and the RF millivoltmeter.

(7) Connect the frequency counter to PL29 and check that it indicates 40 000 000 Hz plus or minus 1Hz. Disconnect the frequency counter and replace the coaxial socket removed from PL29.

(8) Remove the coaxial socket from PL26 on the reference generator board, and connect PL26 to the RF millivoltmeter.

(9) Adjust transformer T2 for a maximum indication on the RF millivoltmeter. Ensure that the level indicated is within plus or minus 3dB of +3dBm.

(10) Connect the digital multimeter between ML11 pin 6 and chassis, and check that it indicates between 1.4 and 6 volts. Disconnect the digital multimeter and the RF millivoltmeter.

(11) Connect the frequency counter to PL26 and check that it indicates 1 400 000 Hz plus or minus 1Hz. Disconnect the frequency counter and replace the coaxial socket removed from PL26.

(12) Switch off and disconnect all test equipment.

SYNTHESIZER BOARD

20. (1) Connect the digital multimeter between TP1 and chassis. Adjust R7 for a d.c. voltage reading of +5.2V plus or minus 50 millivolts. Disconnect the digital multimeter.

(2) Set the MA1723 to a frequency of 15 601.0 kHz and select TUNE.

(3) Connect the oscilloscope, AC coupled, sensitivity 5 millivolts per division, sweep speed 0.2 milliseconds per division, between TP16 and ground (TP17).

(4) Momentarily short TP7 to ground (TP3) and trigger the oscilloscope from TP5.

(5) Adjust R43 for minimum trace amplitude.

(6) Disconnect the oscilloscope.

(7) Set the MA1723 to a frequency of 29 999.9 kHz.

(8) Connect the digital multimeter between TP16 and ground (TP17).

(9) Adjust L11 for +15V d.c. plus or minus 100mV.

(10) Disconnect the digital multimeter.

(11) Set the MA1723 POWER switch to OFF.

MODULATION BOARD

Carrier Level

21. (1) Connect test lead 1, shown in fig. 19(a), to SK4 on the rear panel.

(2) Connect test lead 2, shown in fig. 19(b), to SK6 on the rear panel. Ensure that TB3 pin 1 (READY) is linked to TB3 pin 2 (OV) on test lead 2.

(3) Set the VOX/PTT/TX switch to TX and select the CW mode.

(4) Remove the coaxial socket from PL14 on the modulation board and connect PL14 to the RF millivoltmeter.

(5) Close the KEY switch (connected to test lead 1).

(6) Adjust T5 for a maximum indication on the RF millivoltmeter and then adjust R161 for an indication of 0dBm plus or minus 0.25dB.

(7) Select LOW POWER at front panel and adjust R165 for the required output power level (set at the factory for an indication of -6dB on the RF Millivoltmeter).

(8) Cancel LOW POWER at the front panel.

(9) Open the KEY switch.

USB Adjustments

22. (1) Set R47, R56, and R159 to mid-position, and set switch SA to the AGC ON position.

(2) At the MA1723 front panel, select the USB mode.

(3) Connect the audio signal generator, set for single tone operation at a frequency of 1kHz, and an output level of 0 dBm, to TB1 of test lead 1, pins 1 and 2 (LINE 1 audio input).

(4) Adjust the rear panel LINE 1 control so that the input level to the modulation board is within the AGC range (so that adjusting the level slightly causes no change in the board output level, as indicated by the RF millivoltmeter connected to PL14).

(5) Adjust R159 for an indication on the RF millivoltmeter of 0dBm.

(6) Set switch SA to the AGC OFF position and adjust the audio signal generator level for an indication of -13dBm on the RF millivoltmeter.

(7) Set switch SA to the AGC ON position.

(8) Set R56 fully clockwise (ML4 to maximum gain).

(9) Adjust R47 for an indication of 0dBm on the RF millivoltmeter.

(10) Increase the audio signal generator output level by 13dB.

(11) Connect the digital multimeter between TP3 and ground, and adjust R56 for an indication of 4.50 volts d.c. plus or minus 0.05V on the digital multimeter.

(12) Ensure that the RF millivoltmeter indicates 0dBm plus or minus 1dB.

(13) Increase the signal generator output level by 10dB and ensure that the RF millivoltmeter indicates 0dBm plus or minus 1dB.

(14) Reduce the signal generator output level by 20dB and ensure that the RF millivoltmeter indicates 0dBm plus or minus 1dB.

LSB Adjustments

23. (1) Set R50, R54 and R160 to mid-position, and set switch SB to the AGC ON position.

(2) At the MA1723 front panel, select the LSB mode.

(3) Adjust the audio signal generator output level so that it is within the AGC range (so that adjusting the level slightly causes no change in the board output level, as indicated by the RF millivoltmeter connected to PL14).

(4) Adjust R160 for an indication on the RF millivoltmeter of 0dBm.

(5) Set switch SB to the AGC OFF position and adjust the audio signal generator level for an indication of -13dBm on the RF millivoltmeter.

(6) Set switch SB to the AGC ON position.

(7) Set R54 fully clockwise (ML8 to maximum gain).

(8) Adjust R50 for an indication of 0dBm on the RF millivoltmeter.

(9) Increase the audio signal generator output level by 13dB.

(10) Connect the digital multimeter between TP4 and ground, and adjust R54 for an indication of 4.50 volts d.c. plus or minus 0.05V on the digital multimeter.

(11) Ensure that the RF millivoltmeter indicates 0dBm plus or minus 1dB.

(12) Increase the signal generator output level by 10dB and ensure that the RF millivoltmeter indicates 0dBm plus or minus 1dB.

(13) Reduce the signal generator output level by 20dB and ensure that the RF millivoltmeter indicates 0dBm, plus or minus 1dB. Disconnect the RF millivoltmeter from PL14.

Monitor Amplifiers

24. (1) Ensure that the audio signal generator, set for single tone operation at 1kHz, is connected to TB1 of test lead 1, pins 1 and 2 (LINE 1 AUDIO IN). Set the audio signal generator output level to 0dBm.

(2) Connect the telephone handset to the LINE 1 socket on the front panel. Adjust R29 for the desired output level from the handset earpiece.

(3) Transfer the audio signal generator to pins 4 and 5 of TB1 (LINE 2 AUDIO IN).

(4) Transfer the telephone handset to the LINE 2 socket on the front panel. Adjust R30 for the desired output level from the handset earpiece.

(5) Replace the coaxial socket removed from PL14 and disconnect the audio signal generator.

VOX Adjustment

25. (1) Connect the RF millivoltmeter, via the step attenuator set to 13 dB, to SK2 (RF OUT) on the rear panel.

(2) Connect the audio signal generator, set for single tone operation at 1 kHz, to TB1 of test lead 1, pins 1 and 2.

(3) Set the MA 1723 to a frequency of 15 000.0 kHz, select USB, and set the VOX/PTT/TX switch to VOX.

(4) Set R69 on the modulation board fully clockwise.

(5) Set the LINE/SET/RF switch to the SET position. Adjust the audio signal generator output level for an indication of 0 dBm on the front panel meter.

(6) Ensure that TRANSMIT is indicated in the right-hand display panel, and that the RF millivoltmeter indicates an RF output signal (the RF output level depends on the setting of R1 on the RF output board).

(7) Reduce the audio signal generator output level by 6 dB. Se R69 on the modulation board fully anti-clockwise.

(8) Ensure that the TRANSMIT and RF output indications are no longer present.

(9) Slowly adjust R69 clockwise until the position is just reached where the TRANSMIT and RF output indications reappear.

NOTE: The VOX sensitivity may be increased by reducing the audio signal generator output level by more than 6 dB at step (7). Conversely, the VOX sensitivity may be decreased by reducing the audio signal generator output level by less than 6 dB at step (7).

MIXER BOARD

41.4MHz L-C Filter Alignment

26. (1) Set R26 fully anti-clockwise.

(2) Remove links LK1 and LK2.

(3) Connect the tracking generator output to LK1 B and C (earth). Connect the spectrum analyser input to LK2 A and C (earth).

(4) Set the MA1723 POWER switch to ON.

(5) Set the spectrum analyser/tracking generator as follows:

Output Level	-10dBm
Centre Frequency	41.4MHz
Horizontal Scale	100KHz per division
Vertical Scale	1dB or 2dB per division

(6) Adjust the spectrum analyser to display the filter response and adjust L1, L2 and L3 for a peak at 41.4MHz.

(7) Set the spectrum analyser centre frequency to 38.6 MHz and the vertical scale to 10dB per division. Adjust L2 for a notch at 38.6MHz.

(8) Adjust the spectrum analyser to position the peak of the response at the top of the screen. Ensure that the peak level is not less than -19dBm.

(9) Tune ths spectrum analyser to the following frequencies, in turn, and ensure that the specified attenuation relative to the peak level is obtained.

Frequency	Attenuation (not less than)
38.6 MHz	40dB
42.8 MHz	10dB

(10) Set the MA1723 POWER switch to OFF.

(11) Disconnect the spectrum analyser/tracking generator and replace link LK1.

41.4MHz Crystal Filter Alignment

27. (1) Remove link LK3

(2) Connect the tracking generator output to LK2 B and C (earth).

(3) Connect the spectrum analyser input to LK3 A and C (earth).

(4) Set the MA1723 POWER switch to ON.

(5) Set the spectrum analyser/tracking generator as follows:

Output Level	-10 dBm
Centre Frequency	41.4 MHz
Horizontal Scale	5 kHz per division
Vertical Scale	1 dB or 2 dB per division

(6) Set C20 to mid-position.

(7) Adjust the spectum analyser to display the filter passband. Adjust L4 and L5 for a response within the limits defined in fig.19(j).

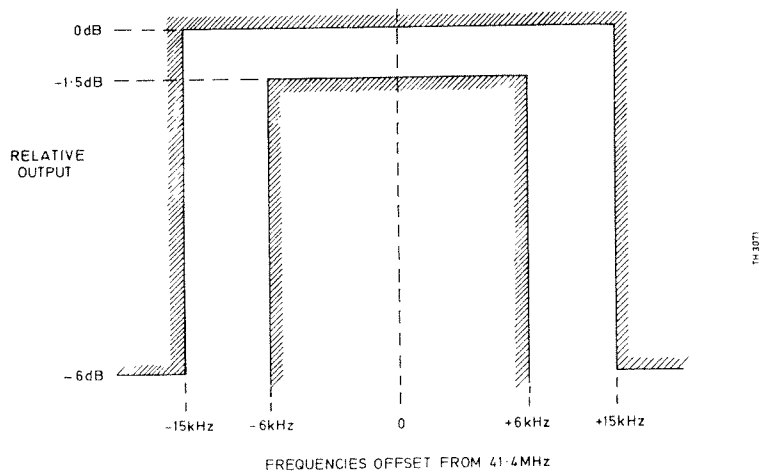


Fig.19(j) Filter Response Limit

(8) Set the spectrum analyser horizontal scale to 500kHz per division, and the vertical scale to 10dB per division.

(9) Adjust C20 for an approximately symmetrical response at plus and minus 1MHz. Ensure that the attenuation at plus and minus 1MHz is not less than 45dB.

NOTE: Any spurious responses on the high frequency side of the passband can be ignored.

(10) Set the MA1723 POWER switch to OFF, disconnect the spectrum analyser/tracking generator and replace links LK2 and LK3.

30MHz Low Pass Filter Alignment

28. (1) Remove link LK4.

(2) Connect the tracking generator output to LK4 B and C (earth).

(3) Remove the coaxial socket from PL20 on the mixer board. Connect PL20 to the spectrum analyser input.

(4) Set the MA1723 POWER switch to ON.

(5) Set the spectrum analyser/tracking generator as follows:

Output level	-10dBm
Centre Frequency	42.8MHz
Horizontal Scale	500KHz per division
Vertical Scale	10dB per division

(6) Adjust the spectrum analyser to display the filter stopband and adjust L10 for a notch at 42.8MHz.

(7) Set the spectrum analyser centre frequency to 46.9MHz. Adjust L9 for a notch at 46.9MHz.

(8) Set the spectrum analyser/tracking generator as follows:

Centre Frequency	25MHz
Horizontal Scale	5MHz per division
Vertical Scale	1dB or 2dB per division

(9) Adjust the spectrum analyser to display the passband and adjust L8 and L11 for minimum loss at 30MHz.

(10) Note the maximum and minimum output levels in the range 1MHz to 30MHz. Ensure that the difference between these levels does not exceed 1.5dB.

NOTE: Allowance must be made for the frequency response of the measuring system. This can be measured by connecting the tracking generator output to the spectrum analyser input. Where the Marconi TF2370 is in use, the calibration response can be stored in memory.

(11) Set the spectrum analyser/tracking generator as follows:

Centre Frequency	50MHz
Horizontal Scale	10MHz per division
Vertical Scale	10dB per division

(12) Adjust the spectrum analyser to display the passband at the top of the screen. Ensure that the output level is not less than +3dBm. Ensure that the stopband attenuation is not less than 70dB from 42.8MHz to 100MHz.

(13) Set the MA1723 POWER switch to OFF, disconnect the spectrum analyser/tracking generator, and replace link LK4.

Mixer Drive Level

29. (1) Set the MA1723 POWER swtich to ON.

(2) Connect the RF millivoltmeter, using the high impedance probe with 20dB attenuator, between TP3 and earth. Ensure that the drive level is 2 volts r.m.s. plus or minus 0.5 volts r.m.s.

(3) Transfer the RF millivoltmeter high impedance probe to TP7, earth to TP8. Ensure that the drive level is 12 volts r.m.s. plus or minus 4 volts r.m.s. Disconnect the RF millivoltmeter.

Overall Gain Adjustment

30. (1) Remove the coaxial socket from PL20 on the mixer board. Connect PL20 to the RF millivoltmeter.

(2) Set the MA1723 to the CW mode and close the KEY switch (connected to test lead 1).

(3) Adjust R26 for an indication on the RF millivoltmeter of +10dBm plus or minus 0.25dB.

(4) Connect the digital multimeter between TP12 and ground. Ensure that it indicates 4.4 volts d.c. plus or minus 1 volt.

(5) Disconnect the RF millivoltmeter and the digital multimeter.

(6) Replace the coaxial socket removed from PL20.

(7) Open the KEY switch.

RF OUTPUT BOARD

31. (1) Connect the RF millivoltmeter, via the step attenuator set to 13dB, to SK2 (RF OUT) on the rear panel.

(2) Set the MA1723 to a frequency of 15 000.0 kHz and select the CW mode.

(3) Set the VOX/PTT/TX switch to TX and close the KEY switch connected to test lead 1.

(4) Adjust R1 on the RF output board for an indication of +10dBm plus or minus 0.25dB on the RF millivoltmeter.

(5) Set the LINE/SET/RF switch to RF and ensure that the front panel meter indicates +23dBm plus or minus 1dB.

NOTE: If an output power level of less than +23 dBm is required, adjust R1 accordingly.

(6) Open the KEY switch (connected to test lead 1).

(7) Disconnect the RF millivoltmeter and step attenuator.

FREQUENCY STANDARD

32. No attempt must be made to adjust the optional internal frequency standard until the drive unit has been operating continuously for at least one hour. Both the 9442 and the 9420 frequency standards have a multi-turn internal trimmer capacitor for adjustment purposes. Access is gained, in each case, by the removal of the rubber plug. The capacitor trim range for the 9442 standard is -6 to +3 parts in 10^6, whilst that for the 9420 trimmer capacitor is -8 to +2 parts in 10^7. The 9420 standard assembly has an additional fine-trim control (R2) which has a trim range of approximately 1 part in 10^7.

NOTE: 1. Ensure that an external standard is not connected to SK3 (EXT REF) on the rear panel, as this will override the output from an internal standard.

2. The following procedure requires the use of an external 1MHz frequency standard which has a higher degree of accuracy and stability then the 9442 or the 9420, as appropriate.

Adjustment Procedure

33. (1) Ensure that an external standard is not connected to SK3 on the rear panel.

(2) Ensure that the drive unit has been running continuously for at least one hour.

(3) Connect the RF monitor socket on the MA1723 front panel to the oscilloscope Channel A input.

(4) Connect the external frequency standard to the oscilloscope Channel B input.

(5) Set the oscilloscope to display Channel A on the vertical axis and Channel B on the horizontal axis.

(6) For the 9420 standard only, set R2 (adjacent to the internal standard) to mid-position.

(7) Set the MA1723 to a frequency of 1 000.0 kHz and select TUNE.

(8) Remove the rubber plug from the frequency standard and, using the trimming tool provided, adjust the internal trimmer for a stable lissajou figure. One rotation of the lissajou figure per second is equal to a 1Hz offset (frequency difference) between the two standards.

(9) Replace the rubber plug.

(10) For the 9420 standard (ensure that the rubber plug has been replaced), adjust R2 for a stable display.

(11) Switch off and disconnect all test equipment.

FSK BOARD (FSK Version only)

34. (1) Connect the test equipment as shown in fig. 19(d). Set the step attenuator to 13dB.

(2) Ensure that LK1 on the FSK board is in position A-D (positive - neutral).

(3) Set the MA1723 to a frequency of 15 000.0 kHz, set the VOX/TX/PTT switch to TX and select the CW mode.

(4) Close the KEY switch (connected to test lead 1) and check that the RF millivoltmeter indicates an RF output signal. Note the level.

(5) Open the key switch and select FSK at the MA1723 front panel.

(6) On the FSK board, remove link LK2 and check that the frequency counter indicates 15 000.000 kHz plus or minus 2Hz. If necessary adjust R20 on the FSK board.

(7) Ensure that the RF millivoltmeter indicates the level noted at step (4) ± 0.5dB. If necessary adjust R28 on the FSK board.

(8) Fit LK2 to the FSK board in position A-C and set the FSK INPUT switch (connected to test lead 1) to the mark (M) position.

(9) Adjust R15 on the FSK board for the required frequency shift, in the range 42Hz to 425Hz (set to 400Hz at the factory), i.e. adjust R15 so that the frequency counter indicates 15 000.000 kHz plus the required frequency shift.

(10) Set the FSK INPUT switch to space (S) and ensure that the frequency counter indicates 15 000.00 kHz minus the required frequency shift.

(11) Connect the telephone handset to the LINE 1 socket the MA1723 front panel.

(12) Alternately set the FSK INPUT switch to M and S and ensure that a change in tone is heard in the telephone handset.

(13) Switch off and disconnect all test equipment.

CHAPTER 20

FAULT DIAGNOSIS

CONTENTS

Tables

Illustrations

CHAPTER 20

FAULT DIAGNOSIS

INTRODUCTION

1. This Chapter provides information to assist in the location of a faulty component or sub-assembly. A series of checks and suggestions are given with references to the self-test routines contained in Chapter 18 and to the functional test routines contained in Chapter 19. Signature analysis tests are given at the end of this chapter.

TEST EQUIPMENT

2. The items of test equipment required are as given in Chapter 19 with the following additional item:

    Signature Analyser
    Hewlett Packard HP5004A

PRELIMINARY

3. If the rear panel connectors, front panel controls and internal switches and connectors are not readily accessible, remove the unit from the rack or cabinet and place it on a flat, clean working surface.

4. If the nature of the fault is unknown, carry out the functional test procedures given in Chapter 19. These make use of some of the built-in test routines detailed in Chapter 18. If a fault is indicated whilst carrying out these routines, or if the routines do not run, refer to the manual tests (with the same respective test numbers) given in this chapter (paras. 7 to 27).

5. If the fault is associated with the optional SCORE interface board, then attempt to run self-test routine number 15 (Chapter 18, para. 35). Similarly, if the fault is associatd with the optional FSK board, then attempt to run self-test routine number 19 followed by 20 (Chapter 20, paras. 42 and 43).

6. If the self-test routines so far attempted do not reveal a fault condition, then further checks of the logic circuitry can be made by running self-test routine number 18 (Chapter 18, para. 41), or by running the signature analysis routines described in paras. 28 to 49. Once the synthesizer circuitry has been checked, an audio signal can be applied to the modulation board, and the signal paths can be traced through the unit using the information provided on the appropriate circuit diagrams.

MANUAL TESTS

7. The following paragraphs detail the manual tests to be made when a fault is indicated whilst carrying out the self-test routines (described in Chapter 18 and called in Chapter 19). For ease of reference, each manual test is given the same number as that of the associated self-test routine.

Test M00/a - Self-Test Does Not Run

8. (1) Check the power supplies on the processor board, as follows:

+5V - Outer end of R3 (near crystal)
+5V UNREG A (approximately +10V) - ML15 pin 8

(2) If either supply is faulty, trace back to the power supply module. If necessary, unplug each relevant board, in turn, to check for a short-circuit.

(3) If the supplies are correct, replace the processor board with a known serviceable spare (it may be necessary to transfer the programmed devices PD1 to PD3), or use the following procedure to locate a fault on the processor board:

(a) Use the oscilloscope to check that the 2MHz processor clock is running (ML1 pin 1)

(b) Check that the supplies are present at the correct pins of each integrated circuit.

(c) Check that the processor $\overline{\text{CLEAR}}$ line (TP6) is at logic '1' (approximately +5V).

(d) Carry out the signature analysis checks detailed in paras. 38 and 39.

(4) If the processor board appears to be functioning correctly, replace the front panel interface board with a known serviceable spare, or carry out manual tests M06 and M07.

(5) If the front panel interface board appears to be functioning correctly, replace the front panel display board with a known serviceable spare, or carry out manual tests M06 and M07.

Test M00/b - Supply Line Fault

9. (1) The particular failed supply line is indicated on the frequency display. Disconnect boards, as appropriate, to check for a short circuit. If the supply output from the power supply module is incorrect with all boards disconnected, replace or repair the power supply module.

NOTE: If more than one supply line is at fault, the first to be detected is displayed, whilst further failures will be displayed, in turn, each time the ENTER pushbutton is pressed and released.

(2) If the supply lines are found to be correct, press and release the ENTER button to proceed from routine 00 and run test routines 01 to 07, as detailed in the flow chart given in Chapter 18.

(3) If self-test routines are completed successfully, replace the front panel interface board with a known serviceable spare, or carry out the following:

(a) Run self-test routine number 18 to check the DAC output at TP26 on the front panel interface board. A smooth rising staircase waveform from 0V to +10V should be displayed.

(b) Check the supply metering attenuator resistors (R8 to R19) on the front panel interface board, which feed the analogue multiplexer device ML11.

(c) Whilst running self-test routine number 00, use the oscilloscope to check the operation of the analogue multiplexer ML11 and the metering comparator ML20, on the front panel interface board.

(d) Carry out the signature analysis routine given in paras. 41 to 44 to check for correct operation of the data bus and strobe inputs to the DAC and metering select circuitry.

Test M01 - ROM Check Sum Fault

10. (1) Replace the processor board or the ROM devices PD1 and PD2.

(2) If the fault persists following ROM replacement, replace the processor board or carry out the following:

(a) Check the supplies to each individual integrated circuit.

(b) Carry out the signature analysis routines given in para. 38, to concentrating on the data bus, address bus and addressing circuitry.

Test M02 - RAM Test 1 Failure

11. Replace the processor board with a known serviceable spare, or carry out the following:

(1) Check the RAM devices ML4 and ML5 by replacement.

(2) Carry out the signature analysis routines given in paras. 38 and 39 to check the RAM input and output circuitry.

Test M03 - RAM Test 2 Failure

12. Replace the processor board with a known serviceable spare, or carry out the following:

(1) Check the RAM devices ML4 and ML5 by replacement.

(2) Carry out the signature analysis routines given in paras. 38 and 39 to check the RAM input and output circuitry.

Test M04 - EAROM Test Failure

13. Replace the processor board or carry out the following:

(1) Check for the correct supplies (+5V, -12V, -30V, 0V) at each of the two EAROM devices.

(2) Carry out the signature analysis routines given in para. 39 to check the EAROM address and data bus lines.

(3) If no faults are found, suspect a faulty EAROM device ML2 and/or ML3.

Test M05 - PIO Test Failure

14. Replace the processor board or carry out the signature analysis routine given in para. 39. Check the PIO and CPU devices, ML9 and ML1, by substitution.

Test M06 - Display Fault

15. Replace the front panel display board with a known serviceable spare, or carry out the following:

(1) Check the power supplies to each integrated circuit.

(2) Check that the nominal 130Hz 5V peak-to-peak display clock signal is present at TP4, at the DF pins on each of the display driver integrated circuits, and at the back plane (BP) connections on the two LCD panels, ML1 and ML11.

(3) Check for correct data at the outputs of the display driver integrated circuits and at the appropriate pins of the respective LCD panel. If the data at these pins is correct and the display is incorrect, then replace the LCD panel.

(4) Carry out the signature analysis routine given in para . 45 to check the data bus, the display driver strobes and the display address lines. If correct signatures are obtained, suspect a faulty display driver device. If incorrect signatures are obtained, suspect ML10 (display driver strobes only incorrect), a faulty front panel interface board, or the connections between the front panel display board and the front panel interface board.

(5) If the front panel interface board is suspect, either replace the board or carry out the following:

(a) Check the power supplies to each integrated circuit associated with the addressing and display counter circuitry.

(b) Carry out the signature analysis routine given in paras. 42 and 43 to trace the data bus back to the processor board connector PL39.

(c) Check for correct signatures around the display counter ML7 and the output data strobe decoder ML9.

Test M07 - Front Panel Switch Test Failure

16. Replace the front panel display board with a known serviceable spare, or carry out the following:

(1) Disconnect SK41 from PL41 on the front panel interface board. Use the multimeter to check that no short circuits are present between switch matrix column inputs and row outputs at SK41 on the front panel display board with no pushbuttons depressed.

(2) Use the multimeter to check for continuity between the appropriate column input and row output for each front-panel pushbutton (when depressed).

(3) If no fault is found, replace the front panel interface board, or carry out the following:

(a) Carry out the signature analysis routine given in Para. 44 to check the input strobe decoding on the front panel interface board (ML1, ML5, ML6) and the data bus connections to the tri-state parallel input buffers (ML12, ML13). If correct signatures are found, suspect a faulty input buffer, ML12 and/or ML13.

Test M08 - Reference Board Test Failure

17. (1) Ensure that either:

(a) The unit is fitted with an internal frequency standard module.

or

(b) that a suitable external frequency standard is connected to SK3 (EXT REF) on the rear panel.

(2) Replace the reference generator board, or carry out the following:

(a) Run self-test routine 08 and use the ENTER pushbutton to determine whether more than one fault is indicated.

(b) Refer to the fault code given in Chapter 18, para. 19 and then carry out measurement checks on the reference generator board, with reference to the circuit diagram (Chapter 7, fig.7.1).

(c) If the 20 MHz varactor voltage is out of range, use the oscilloscope to check the internal/external reference interface circuits and the 20MHz phase-locked loop.

(d) If the 1.4 MHz output signal is incorrect, check the divide-by-100 stage (ML12, ML13), the 1.4MHz crystal filter (XL2, XL3), and the output amplifierr stage (TR6, TR7).

(e) If the 40MHz output signal is incorrect, check the frequency double stage (TR5, T3).

Test M09 - Synthesizer Test Failure

18. (1) Ensure that the 20 MHz reference signal is present at PL32 on the synthesizer board.

(2) Replace the synthesizer board, or carry out the following:

(a) Run self-test routine 09 to determine the fault code. Refer to Chapter 18, para. 22 for an interpretation of the fault code and then carry out measurement checks on the synthesizer board, with reference to the circuit diagrams (Chap 8, figs. 8.1 and 8.2).

(b) If the varactor voltage is out of range at 0 or 30 MHz, press and release the RCL pushbutton, and set the drive unit to a frequency of 30 MHz. Adjust L11 on the synthesizer board for a varactor line voltage of 15V d.c. at TP16. Ensure that the synthesizer functions correctly over the entire frequency range, and check that at 0 MHz, the varactor line voltage level at TP16 is not less than 3V d.c.

(c) If the synthesizer is not functioning correctly, check the power supplies to each integrated circuit.

(d) Carry out the signature analysis routine given in para. 47 to check data bus inputs DB0 to DB4 and output strobe OP29 at TP4. If incorrect signatures are obtained, trace the data bus and OP29 lines back to the front panel interface board.

(e) If no fault is found, run self-test routine number 21, the synthesizer board signature analysis routine, in conjunction with paras. 48 and 49.

(f) Use the oscilloscope to check the 20MHz reference input circuitry, the 42.4 MHz to 71.4 MHz VCO (TR8), the VCO buffer amplifier (TR1, TR2, TR3), the programmed divider and the phase-locked loop.

Test M10 - Modulation Board USB Failure

19. Replace the modulation board with a known serviceable spare (carry out a functional check and re-align the replacement board, if necessary), or carry out the following:

(1) Run self-test routine number 10 and establish the nature of the fault with reference to the fault code information given in Chapter 18, para. 24.

(2) Check that the power supply voltages are present and correct on the modulation board.

(3) Check for correct operation of the sidetone oscillator ML31.

(4) Carry out the signature analysis routine given in para. 46 to check the data bus, together with the strobe inputs to, and the data outputs from, latches ML19, ML20, ML21, ML22 and ML29. Alternatively, use the oscilloscope to check for correct data latch operation whilst running self-test routine number 18.

(5) Connect the audio signal generator to the LINE 1 audio input connection of SK4 on the rear panel (use Test Lead 1 described in Chapter 19). Set the audio signal generator to a frequency of 1 KHz and an output level of 0dBm.

(6) At the MA1723 front panel, select USB and set the VOX/PTT/TX switch to TX. Ensure that READY and TRANSMIT are indicated (test leads 1 and 2 must be connected to the unit).

(7) At the MA1723 front panel, set the LINE/SET/RF switch to the LINE position and ensure that the front panel meter display indicates approximately 0dBm. If not, check the operation of the metering circuitry on the modulation board and the front panel interface board.

(8) Ensure that the 1.4 MHz signal is present at PL15 on the modulation board and that the level of the RF drive signal applied to the balanced modulator transformer T1 (from TR3) is approximately 5 V pk-pk.

(9) Use the oscilloscope to trace through the USB signal path on the modulation board. Adjust the LINE 1 level control on the rear panel, as necessary. Refer to the circuit diagram for typical signal and voltage levels.

(10) If necessary, carry out the alignment instructions, for the modulation board given in Chapter 19, paras. 21 to 25.

Test M11 - Modulation Board LSB Failure

20. Replace the modulation board with a known serviceable spare (carry out a functional check and re-align the replacement board, if necessary) or check the LSB signal path as given in para. 19 for the USB signal path (transfer the audio signal generator to the LINE 2 audio input connections and select ISB1).

Test M12 - Modulation Board Carrier Failure

21. Replace the modulation board with a known serviceable spare (carry out a functional check and re-align the replacement board, if necessary), or carry out the following:

(1) Press and release the RCL pushbutton to return the unit to the normal operating mode.

(2) Connect Test Lead 1 (Chapter 19) to SK4 and Test Lead 2 to SK6 on the rear panel.

(3) At the front panel, select the CW mode, set the frequency to 15 MHz, and set the VOX/PTT/TX switch to TX.

(4) Close the KEY switch (connected to Test Lead 1).

(5) Monitor test point TP9 on the modulation board using the digital multimeter and check that it indicates approximately +10V.

(6) Use the oscilloscope to check the carrier amplifier (ML1a, ML1b), the carrier level detector (ML1c, TR7), and the control loop circuitry (ML11, ML12, ML13).

(7) The operation of the sample and hold circuit may be checked using self-test routine number 18.

Test M13 - Mixer Board Test Failure

22. (1) Check that the following input signals are present on the mixer board:

(a) PL17 - 1.4 MHz

(b) PL18 - 40 MHz

(c) PL19 - 42.4 MHz to 71.4 MHz

(2) Replace the mixer board or carry out the following:

(a) Check that the power supply voltages are present and correct on the mixer board.

(b) Trace the signals through the mixer board using the spectrum analyser, RF millivoltmeter or the oscilloscope. Refer to the circuit diagram for typical signal and voltage levels.

(c) If necessary, re-align the mixer board as given in Chapter 19, paras. 26 to 30.

Test M14 - RF Output Board Test Failure

23. (1) Check that the board input signal is present at PL22 on the RF output board.

(2) Replace the RF output board with a known serviceable spare, or carry out the following:

(a) Check that the power supply voltages are present and correct on the RF output board.

(b) Check the operation of the +20V Supply Switching Transistor TR4.

(c) Check the operation of the RF output level detector ML1.

(d) Trace the signal through the board using the RF millivoltmeter or the oscilloscope.

Test M15 - SCORE Interface Test Failure

24. Replace the SCORE interface board, or carry out the following:

(1) Check that the power supply voltages are present and correct on the SCORE interface board.

(2) Whilst running self-test routine number 15, use the oscilloscope to check the operation of the SCORE send and receive circuits.

Test M16 - CW Keying Test Failure

25. Replace the modulation board, or carry out the following:

(1) Enter and run self-test routine number 16.

(2) Whilst the routine is running, use the oscilloscope to check the carrier ON/OFF logic, sample and hold, carrier ON/OFF switch, keying envelope shaper, and carrier level control circuitry on the modulation board.

Test M17 - Linear Amplifier Control Test Failure

26. (1) Ensure that a correctly made test plug is connected to SK6 on the rear panel (see fig. 19(c) in Chapter 19).

(2) Set the MA1723 POWER switch to OFF.

(3) Disconnect SK43 from PL43 on the front panel interface board.

(4) Using the digital multimeter, check for continuity between the following connections on SK43:

Pin 20 to pin 12
Pin 19 to pin 11
Pin 18 to pin 14
Pin 17 to pin 13

(5) If no fault is found, replace the front panel interface board, or carry out the following:

(a) Whilst running self-test routine number 17, use the oscilloscope to check the operation of latch ML14, transistors TR3 to TR6, and NAND drivers ML16, ML17, ML18, on the front panel interface board.

(b) Carry out the signature analysis routine given in paras. 43 and 44 to check the data bus, strobe lines and connections to ML14, ML16, ML17, ML18 (on the front panel interface board).

Test M10 - FSK Keying Test Failure

27. Replace the FSK board, or carry out the following:

(1) Whilst running self-test routine number 19, use the oscilloscope to check the key input circuit, the trapezoidal shaper, the oscillator, and the output divider circuitry on the FSK board.

(2) If necessary, re-align the FSK board as detailed in Chapter 19, para. 35.

SIGNATURE ANALYSIS

28. When the MA1723 is operating correctly, the non-sequential program instructions cause continuously changing data patterns to be present within the logic circuitry. Because these data patterns are continuously changing, data analysis or data checking using conventional test equipment (oscilloscopes, logic probes, etc.) becomes almost impossible. The signature analysis technique requires the processor to continuously execute a single instruction (or continuously run a short test program) and so produce repetitive data patterns at selected data nodes throughout the logic circuitry. If the signature analyser START, STOP, CLOCK and GROUND leads are connected to the appropriate test points on a known serviceable unit, and the signature analyser probe is connected in turn, to a number of circuit nodes, then a series of unique 4-digit alpha-numeric 'signatures' will be obtained. If these signatures are recorded, they may be used at a later date as a reference when the same tests are made during the test or fault location procedures. If an incorrect signature is found at a particular node, the operator simply traces back through gates, memory devices, etc until an element with a correct signature at the input and a faulty signature at the output is isolated.

29. The MA1723 contains four signatures analysis routines for testing various parts of the unit, and these are described in the following paragraphs.

Signature Analysis Routines

30. Three of the four signature analysis routines, designated SA1, SA2 and SA3, are selected by first setting the front panel POWER switch to OFF, setting the processor board DIL switches SA to SF to the appropriate positions given below, and then returning the POWER switch to ON. The fourth signature analysis routine is included with the self-test routines, as number 21, and is described in para. 48.

Processor Board DIL Switch Settings

FUNCTION SELECTED	DIL SWITCH					
	C	D	E	F	B	A
NORMAL	O	O	O	O	O	O
SA1	C	O	O	O	O	O
SA2	O	C	O	O	O	O
SA3	O	C	C	O	O	O

O denotes Open (Down)
C denotes Closed (Up)

Routine SA1

31. Closure of test switch SA on the processor card causes the CPU to continuously cycle through the entire address field and to read onto the data bus the data found at each addressed location. This routine is used to check the CPU device (ML1), and the connections between it and other devices on the processor board. The procedure is given in para. 38.

Routine SA2

32. This routine is used to test the RAM, PIO and clock/timer circuitry on the processor board. The procedures are given in para. 39.

Routine SA3

33. This multi-purpose routine is used to test various parts of the front panel display board, the front panel interface board, the modulation board and the synthesizer board. The procedures are given in paras. 40 to 47.

Use of Signature Analyser

34. The type of signature analyser required to carry out the procedures given in this chapter has an integral logic probe which may be used as a test instrument independently of the signature measuring capability. The logic probe incorporates a lamp, and this may be used to indicate one of the following four conditions:

(1) Probe lamp OFF (L) - Logic '0' (GND)

(2) Probe lamp ON (H) - Logic '1'

(3) Probe lamp half ON - High Impedance/poor logic level

(4) Probe lamp flashing (F) - Data stream

35. The signature analyser has START, STOP and CLOCK inputs for connection to the circuit under test, and a logic probe for connection to a circuit node to obtain a signature. The logic levels at the START, SOP and logic probe inputs are strobed into the signature analyser on either the rising or falling edge of the CLOCK input (as selected by the CLOCK pushbutton). Either rising or falling edges of the START and STOP inputs may be selected to initiate and terminate a time period (window or gate) during which measurement takes place.

36. When the START, STOP, CLOCK and GROUND connections are made correctly and the signature analysis routine is being executed, the GATE indicator should flash. The correct configuration for a particular test can be verified by checking the logic '1' signature, obtained by connecting the probe tip to the positive supply.

37. If the HOLD pushbutton is depressed, the instrument will hold a single one-time signature. The probe can then be removed from the test node whilst the signature comparison is made. The displayed signature is reset by pressing and releasing the RESET button on the probe.

Routine SA1 Procedures (Processor CPU and ROM)

38. (1) Set the front panel POWER switch to OFF.

(2) On the processor board, set switch SA to the closed (UP) position, and ensure that the remaining switches, SB to SF, are all in the open (down) position.

(3) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	IN (negative edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(4) Connect the signature analyser leads to the processor board as follows:

START	TP4
STOP	TP5
CLOCK	TP1
GROUND	Lower end of R2 (0V)

(5) Set the MA1723 POWER switch to ON, and then connect the signature analyser probe, in turn, to any convenient +5V pin (e.g. ML1 pin 40), and to 0V, and check that the following signatures are obtained.

+5V	5FU8
0V	0000

(6) Connect the signature analyser probe, in turn, to the points given in Tables 1 and 2, and check that correct signatures are obtained.

NOTE 1: The signatures on data bus lines D0 to D7 are dependent on the version and issue number of the program contained in ROM devices PD1, PD2 and PD3. The correct signatures may be obtained from a known working unit fitted with the same program.

NOTE 2: Incorrect signatures on the data bus lines D0 to DC7 could be due to a faulty integrated circuit device connected to the data bus. With the exception of ML1, PD1, PD2 and PD3, any other integrated circuit connected to the data bus may be removed without affectinng the correct bus signatures.

Routine SA2 Procedures (Processor RAM and PIO)

39. (1) Set the front panel POWER switch to OFF, disconnect SK40 from PL40 on the processor board, release the four captive screws securing the processor board, and lift the board out of the unit, to hinge on the ribbon cable SK39 to PL39 on the front panel interface board.

(2) On the processor board, set switch SB to the closed (UP) position, the remaining switches, SA and SC to SF, to the open (down) position.

(3) At the MA1723 front panel, set the LINE/SET/RF switch to SET, and set the VOX/PTT/TX switch to TX.

(4) Set the signature analyser controls as follows:

Table 1: Processor Input and Output Signatures

SIGNAL	TEST POINT	SIGNATURE	
VCC	ML1 pin: 16	C690	INPUTS
VDD	40	C690	
VSS	20	0000	
$\overline{\text{CLEAR}}$	3	C690	
$\overline{\text{WAIT}}$	2	C690	
$\overline{\text{CLOCK}}$	1	C690F	
$\overline{\text{DMA IN}}$	38	C690	
$\overline{\text{DMA OUT}}$	37	0000	
$\overline{\text{INT}}$	36	C690	
TPA	34	0000F	OUTPUTS
TPB	33	0000F	
SC0	6	0000	
$\overline{\text{SC1}}$	5	C690	
$\overline{\text{MRD}}$	7	0000F	
$\overline{\text{MWR}}$	35	C690	

F denotes flashing probe

Table 2: Processor Board ROM and Timing Signatures

SIGNAL	SIGNATURE	TEST POINT (IC PIN No.)														
		ML1	ML7	ML8	ML11	ML12	ML13	ML14	PD1	PD2	ML17	ML9	ML4	ML5	ML2	ML3
A0	3457	25				0000			10	10						
A1	13FH	26				04HU			9	9						
A2	50F3	27					50F31		8	8						
A3	411H	28					411H2		7	7						
A4	7233	29				1180	72333		6	6						
A5	P37H	30				755U	P37H4		5	5						
A6	9FFA	31				0000(F)	9FFA16		4	4						
A7	14P7	32					14P715		3	3						
TPA	0000F	34		11			17				11	1				
MRD	0000F	7	15					12	22	22		39	18	18		
AV	0000F		6	2			5,6									
MWR	5FU8	35						11					20	20		
0V	0000(F)	20	8	7	8	8	9	7	14	14	10	20	8	8		
+5V	5FU8	16,40	16	14	16	16	18	14	1,28	1,28	20	40	22	22		
A8	6510								25	25	19				5	5
A9	A623								24	24	18				6	6
A10	808P								21	21	17				7	7
A11	7079								23	23	16				8	8
A12	A82C								2	2	15					
A13	2964								26	26	14					
A14	64HU					2					13					
A15	1180					3					12					
Y0	755U					4			20							
Y2	4H78					6				20						
Y3	5FU8				1	7										
XTAL	0000F	39														
D.CK	0000F		2	3												
AR	0000F		5	4												
MRD.MWR	0000		9					10								

START pushbutton	OUT (positive edge)
STOP pushbutton	IN (negative edge
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(5) Connect the signature analyser leads to the processor board as follows:

START	TP8
STOP	TP8
CLOCK	TP1
GROUND	Lower end of R2 (0V)

(6) Set the MA1723 POWER switch to ON, and then connect the signature analyser probe, in turn, to any convenient +5V pin (e.g. ML1 pin 40), and to 0V, and check that the following signatures are obtained:

+5V	9A1A
0V	0000

(7) Check that the RUN/FAULT LED D1 on the processor board is flashing dimly approximately at the rate of two flashes per second.

(8) Connect the signature analyser probe, in turn, to the test points given in Table 3 and check that correct signatures are obtained.

(9) Set the MA1723 POWER switch to OFF.

(10) At the signature analyser, set the START pushbutton to the IN (logic '0') position, and set the STOP pushbutton to the OUT (logic '1') position.

(11) Set the MA1723 POWER switch to ON, and then connect the signature analyser probe, in turn, to any convenient +5 V pin (e.g. ML1 pin 40), and to 0 V, and check that the following signatures are obtained:

+5 V	UU83
0 V	0000

(12) Connect the signature analyser probe, in turn, to the test points given in tables 4 and 5, and check that correct signatures are obtained.

(13) Set the MA1723 POWER switch to OFF, disconnect the signature analyser leads, and return the processor board to the unit.

Table 3: Processor Board RAM Signatures

SIGNAL	SIGNATURE	TEST POINT (IC PIN No.)						
		ML1	ML13	ML4	ML4	ML11	ML14	ML9
$\overline{EF1}$	0000	24	-	-	-	-	-	-
$\overline{CS3}$	9A1A	-	10	-	-	14	-	-
$\overline{CS2}$	9A1A	-	11	-	-	12	-	-
$\overline{CS0}$	H5P2	-	13	-	-	-	2	-
A0	62A1	-	-	4	4	-	-	-
A1	PP5H	-	-	3	3	-	-	-
A2	5U27	-	-	2	2	-	-	-
A3	2HFH	-	-	1	1	-	-	-
A4	3118	-	-	21	21	-	-	-
A5	FAFA	-	-	5	5	-	-	-
A6	1827	-	-	6	6	-	-	-
A7	CU3P	-	-	7	7	-	-	-
$\overline{CS1}$	H5P2	-	-	19	19	-	1	-
CS2	9A1A	3	-	17	17	-	13	13
R/$\overline{W}$	6FA0	35	-	20	20	-	11	-
0D	49UC	7	-	18	18	-	12	39
D0	6U0U	15	-	-	9,10	-	-	-
D1	3462	14	-	-	11,12	-	-	-
D2	A59A	13	-	-	13,14	-	-	-
D3	2548	12	-	-	15,16	-	-	-
D4	450P	11	-	9,10	-	-	-	-
D5	67C4	10	-	11,12	-	-	-	-
D6	A4FC	9	-	13,14	-	-	-	-
D7	8P98	8	-	15,16	-	-	-	-

Table 4: Processor Board PIO Signatures

SIGNAL	SIGNATURE	TEST POINT (COMPONENT PIN No.)				
		ML9	ML1	ML8	SK39	PL40
'B' STROBE	0000	17	-	-	-	-
'A' READY	0000F	36	-	9	-	-
$\overline{\text{CLEAR}}$	UU83	13	3	-	-	9
'A' STROBE	6FF4	35	-	13	-	-
D0	510U	5	15	-	-	-
D1	07PA	6	14	-	-	-
D2	71AA	7	13	-	-	-
D3	3CU7	8	12	-	-	-
D4	53A7	9	11	-	-	-
D5	88F0	10	10	-	-	-
D6	H223	11	9	-	-	-
D7	6PAU	12	8	-	-	-
$\overline{\text{STROBE}}$	9347	-	-	12	9	-
$\overline{\text{WR}}/\overline{\text{RE}}$	0000F	38	33	10	-	-
$\overline{\text{RD}}/\overline{\text{WE}}$	0FF8	39	7	-	-	-

Table 5: Procesor Board Clock/Timing Signatures

SIGNAL	SIGNATURE	TEST POINT (COMPONENT PIN No.)			
		ML1	ML6	ML9	ML8
CLOCK	0000F	33	10	37,38	10
RESET	0000	-	11	-	-
$\overline{\text{INT}}$	UU83	36	-	-	-
$\overline{\text{EF4}}$	UU83	21	-	-	-
TPA	0000F	34	-	1	11
$\overline{\text{MRD}}$	0FF8	7	-	39	-
$\overline{\text{CLEAR}}$	UU83	3	-	13	-
N0	9889	19	-	3	-
N1	4101	18	-	4	-
N2	4101	17	-	2	-

Routine SA3 Procedure (Multi-purpose)

40. Routine SA3 is divided into six parts as follows:

A - Port Address Line Decoding (Para. 42)
B - Output Port Strobe Lines and Data Bus (Para. 43)
C - Input Port Strobe Lines and Data Bus (Para. 44)
D - Display Board (Para. 45)
E - Modulation Board (Para. 46)
F - Synthesizer Board Input Data (Para. 47)

Preliminary

41. (1) Set the MA1723 POWER switch to OFF

(2) Set switches SB and SF on the processor board to the closed (UP) position, and set the remaining switches, SA, SC, SD and SE, to the open (down) position.

(3) Remove the four screws securing the front panel to the front panel assembly, two screws at each edge (not the two recessed screws), and remove the front panel.

(4) Remove the remaining two screws securing the front panel assembly to the unit. Gently ease the front panel assembly forward and lower to 'hinge' on the connecting cableforms.

NOTE: Support the edges of the lowered front panel assembly to prevent inadvertant operation of any of the front panel pushbutton switches.

(5) Disconnect the socket mating with PL40 on the processor board (if fitted).

(6) Disconnect the FSK board (if fitted) from PL46 on the rear panel board.

(7) On the modulation board, set the USB and LSB AGC switches SA and SB to the open (off) position, i.e. towards the edge of the board.

(8) Ensure that no external connections are made to SK4 or SK6on the rear panel, and that no connections are made to the front panel LINE 1 and LINE 2 sockets.

(9) At the front panel, set the LINE/SET/RF switch to SET, and set the VOX/PTT/TX switch to PTT.

(10) Set the signature analyser controls as follows:

START pushbutton	OUT (positive edge)
STOP pushbutton	IN (negative edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(11) Connect the signature analyser leads as follows:

START	ML5 pin 12, front	
STOP	Panel interface board	
CLOCK	TP1	On the processor
GROUND	Lower end of R2	board

(12) Temporarily raise the front panel assembly, set the POWER switch to ON, and check that the front panel displays are as given in Fig. 20(a).

(13) Check that the STANDBY and EHT LED indicators are flashing rapidly.

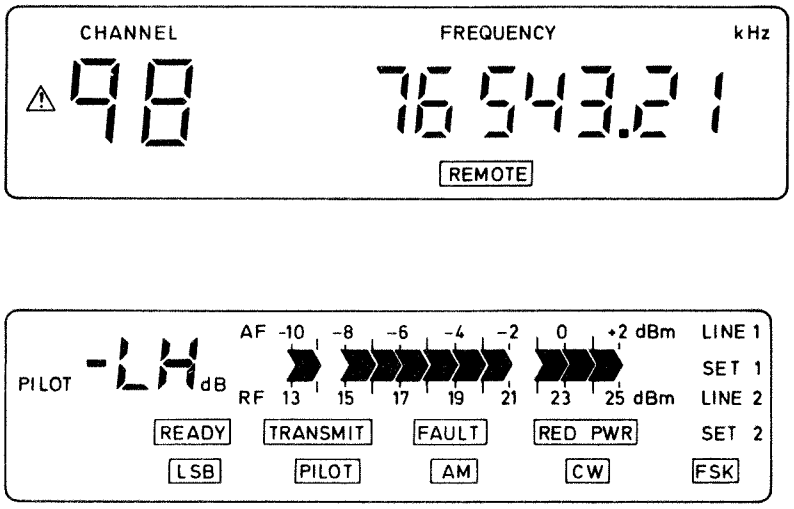


Fig. 20(a) Routine SA3 Front Panel Displays

(14) Connect the signature analyser probe in turn, to the following points on the front panel interface board and check that correct signatures are obtained.

+5V	- Positive end of C1	-	82CP
0V	- Negative end of C1	-	0000

Routine SA3A - Port Address Line Decoding

42. (1) Connect the signature analyser probe, in turn, to the points on the front panel interface board given in Table 6 and check that correct signatures are obtained.

Table 6: Routine SA3A Signatures

SIGNAL	SIGNATURE	TEST POINT (COMPONENT PIN No.)					
		PL39	ML6	ML9	ML5	ML1	TP1
PA0	6HU0	15	11	2	-	-	-
PA1	58H6	14	10	3	-	-	-
PA2	270U	13	9	21	-	-	-
PA3	0000F	12	-	22	-	-	-
PA4	82CPF	11	-	-	12	8	-
PA6	0000	5	-	-	2	-	-
PA7	0000	4	-	-	1	-	-
STROBE	4709	9	3	-	-	9,1	TP1
+5V	82CP	27	16	1	13	14	-
INHA	0000F	-	6	-	-	13,4	-
INHB	82CPF	-	-	23	-	13,4	-
ML5/3	0000	-	-	-	3	5	-
ML5/11	0000F	-	-	-	11	6	-
ML1/3	4497	-	-	-	-	3,12	-

Routine SA3B - Output Strobe Lines & Data Bus

43. (1) Set the signature analyser controls as follows:

START pushbutton	IN (logic '0')
STOP pushbutton	OUT (logic '1')
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(2) Set the MA1723 POWER switch to OFF.

(3) Connect the signature analyser leads as follows:

START	ML5 pin 12,
STOP	Front panel interface board
CLOCK	TP1 Processor
GROUND	Lower end of R2 Board

(4) Ensure that:

(a) Switches SB and SF on the processor board are both set to the closed (UP) position.

(b) Switches SA, SC, SD and SE on the processor board are set to the open (down) position.

(c) The AGC switches SA and SB on the modulation board are both set to the open (off) position, i.e. towards the edge of the board.

(d) The LINE/SET/RF switch is set to the SET position.

(e) The VOX/PTT/TX switch is set to the PTT position.

(5) Set the MA1723 POWER switch to ON.

(6) Connect the signature analyser probe, in turn, to the points on the front panel interface board given below and check that correct signatures are obtained.

+5V - Positive end of C1 - 8U93
0V - Negative end of C1 - 0000

(7) Connect the signature analyser probe, in turn, to the points given in Tables 7 and 8, and check that correct signatures are obtained. Incorrect signatures on the DB0 to DB7 lines may be due to a faulty integrated circuit device connected to the data bus. As an aid to fault location, any integrated circuit device on the front panel interface board connected to the data bus may be removed without affecting the correct bus signatures. The front panel display board, modulation board and synthesizer board may also be disconnected.

Table 7: Routine SA3B Signatures 1

SIGNAL	SIGNATURE	TEST POINT (COMPONENT PIN No.)									
		ML10	ML3	ML14	ML8	ML7	SK31	SK25	SK12	PL39	PL41
DB0	UUOF	1	4	3	3	4	2	2	10	19	10
DB1	HP49	2	7	4	4	12	1	1	13	20	13
DB2	5319	3	13	6	6	13	3	3	14	21	14
DB3	9UPP	4	14	11	11	3	5	5	15	22	15
DB4	C646	5	-	13	13	-	6	-	11	23	11
DB5	HA85	6	-	14	14	-	-	-	12	24	12
DB6	6U62	7	-	-	-	-	-	-	17	25	17
DB7	UOUA	8	-	-	-	-	-	-	16	26	16
+5V	8U93	-	16	16	16	16	20	20	37	27	21
N0	93H2	-	-	-	-	6	-	-	-	-	
N1	9H03	-	-	-	-	11	-	-	-	-	
N2	U891	-	-	-	-	14	-	-	-	-	
N3	24H7	-	-	-	-	2	-	-	-	-	

Table 8: Routine SA3B Signatures 2

SIGNAL	SIGNATURE	TEST POINT (IC PIN No.)								
		ML3	ML4	ML5	ML7	ML8	ML9	ML10	ML11	ML14
TP11	00H3	-	-	8	-	-	11	-	-	-
TP13	8UUC	5	-	-	-	-	15	-	-	-
TP14	32C1	-	-	-	-	-	14	-	-	-
TP15	4716	-	-	-	-	-	19	-	-	-
TP16	F55C	-	-	-	-	-	20	-	-	-
TP17	P03H	-	-	-	-	-	17	-	-	-
TP18	9ACA	-	-	-	-	-	4	-	-	-
TP19	87C9	-	-	-	-	9	6	-	-	-
TP20	PCF1	-	-	-	-	-	7	-	-	9
TP21	A5P8	-	-	6	-	-	10	-	-	-
TP22	1208	-	-	-	1	-	9	-	-	-
+5V	8U93	6	1,15	5,9	10	1	24	-	-	16
$\overline{CE}$	2A7C	-	-	4	-	-	-	9	-	-
$\overline{CS}$	0000	-	-	-	-	-	-	10	-	-
+VCC	8U93	-	-	-	-	-	-	11	-	-
Q1	853P	2	3	-	-	-	-	-	-	-
Q2	4902	10	6	-	-	-	-	-	-	-
Q3	331C	11	10	-	-	-	-	-	-	-
Q4	F251	1	14	-	-	-	-	-	-	-
ST	8U40	-	-	10	15	-	-	-	-	-
A	853P	-	4	-	-	-	-	-	10	-
B	4902	-	5	-	-	-	-	-	11	-
C	331C	-	11	-	-	-	-	-	14	-
D	F251	-	13	-	-	-	-	-	13	-

Routine SA3C - Input Port Strobe Lines and Data Bus

44. (1) Set the signature analyser controls as follows:

START pushbutton	OUT (positive edge)
STOP pushbutton	IN (negative edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(2) Set the MA1723 POWER switch to OFF.

(3) Connect the signature analyser leads as follows:

START	ML5 pin 12, Front panel interface board
STOP	
CLOCK	TP1 Processor board
GROUND	Lower end of R2

(4) Ensure that:

(a) Switches SB and SF on the processor board are both set to the closed (UP) position.

(b) Switches SA, SC, SD and SE on the processor board are set to the open (down) position.

(c) The AGC switches SA and SB on the modulation board are both set to the open (OFF) position i.e. towards the board edge.

(d) The LINE/SET/RF switch is set to the SET position.

(e) The VOX/PTT/TX switch is set to the PTT position.

(5) Set the MA1923 POWER switch to ON.

(6) Connect the signature analyser probe, in turn, to the points on the front panel interface board given below and check that correct signatures are obtained:

+5V - Positive end of C1 - 82CP
0V - Negative end of C1 - 0000

(7) Connect the signature analyser, in turn, to the points given in Table 9 and check that signatures are obtained. Any output latch connected to the DB0 - DB7 lines may be removed without affecting the correct bus signatures. Input devices however, must not be removed.

Table 9: Routine SA3C Signature

SIGNAL	SIGNATURE	TEST POINT (IC PIN No.)								
		ML2	ML6	ML12	ML13	ML15	ML16	ML17	ML18	ML19
ROW 7	82CP	-	-	-	2	-	-	-	-	-
ROW 6	82CP	-	-	-	4	-	-	-	-	-
ROW 5	82CP	-	-	-	6	-	-	-	-	-
ROW 4	82CP	-	-	-	10	-	-	-	-	-
ROW 3	82CP	-	-	2	-	-	-	-	-	-
ROW 2	82CP	-	-	4	-	-	-	-	-	-
ROW 1	82CP	-	-	6	-	-	-	-	-	-
ROW 0	82CP	-	-	10	-	-	-	-	-	-
TP12	4497	-	-	1	1	-	-	-	-	-
TP25	CFHH	1,15	1	15	-	-	-	-	-	
TP24	64U4	-	5	-	15	1,15	-	-	-	
TP23	CFU2	-	4	-	-	-	-	-	-	
TR1 COL	3P4F	-	-	-	-	-	2,7	2,7	2,7	
EXT.PTT	82CP	-	-	-	-	-	-	-	-	1,2
EXT.MUTE	82CP	-	-	-	-	-	-	-	-	6,7

Table 9 (Cont'd)

SIGNAL	SIGNA-TURE	TEST POINT (IC PIN No.)								
		ML2	ML6	ML12	ML13	ML15	ML16	ML17	ML18	ML19
$\overline{\text{EXT.PTT}}$	0000	-	-	-	-	12	-	-	-	-
$\overline{\text{EXT.MUTE}}$	0000	-	-	-	-	14	-	-	-	5
RF SW	82CP	-	-	14	-	-	-	-	-	-
LINE SW	82CP	-	-	12	-	-	-	-	-	-
VOX SW	82CP	-	-	-	-	2	-	-	-	-
TX SW	82CP	-	-	-	-	4	-	-	-	-
LSB AGC	82CP	-	-	-	12	-	-	-	-	-
USB AGC	82CP	-	-	-	14	-	-	-	-	-
DB0	5AC8	-	-	9	-	9	-	-	-	-
DB1	5AC8	-	-	7	-	13	-	-	-	-
DB2	CFU2	11	-	5	-	-	-	-	-	-
DB3	8291	13	-	3	-	-	-	-	-	-
DB4	64HC	3	-	-	9	-	-	-	-	-
DB5	64HC	5	-	-	7	-	-	-	-	-
DB6	CFHH	7	-	-	11,5	-	-	-	-	-
DB7	CFHH	9	-	-	13,3	-	-	-	-	-
VOX	0000	-	-	-	-	6	-	-	-	-

Routine SA3D - Display Board

45. (1) Set the MA1723 POWER switch to OFF.

(2) Lower the MA1723 front panel assembly (as detailed in para. 41(3) and 41(4).

(3) Remove the nine screws, each with a crinkle washer, securing the front panel interface board to the front panel assembly.

(4) Disconnect the coaxial socket from PL59 on the front panel interface board.

(5) Raise the front panel interface board to reveal the front panel display board.

(6) Place a sheet of card or other insulating material between the underside of the raised front panel interface board and the exposed stand-off pillars securing the front panel display board.

(7) Connect the signature analyser leads as follows:

START	ML5 pin 12, Front
STOP	Panel interface board
CLOCK	TP1 Processor
GROUND	Lower end of R2 board

(8) Ensure that:

(a) Switches SB and SF on the processor board are both set to the closed (UP) position.

(b) Switches SA, SC, SD and SE on the processor board are set to the open (down) position.

(c) The AGC switches SA and SB on the modulation board are both set to the open (OFF) position.

(d) The LINE/SET/RF switch is set to the SET position.

(e) The VOX/PTT/TX switch is set to the PTT position.

(9) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	OUT (positive edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(10) Set the MA1723 POWER switch to ON.

(11) Connect the signature analyser probe, in turn, to the following points on the front panel display board and check that correct signatures are obtained.

+5V - Positive end of C1 - 8U93
0V - Negative end of C1 - 0000

(12) Connect the signature analyser probe, in turn, to the points given in tables 10, 11 and 12, and check that correct signatures are obtained. Any display driver integrated circuit may be removed without affecting the correct signatures.

(13) Set the front panel POWER switch to OFF.

(14) Re-assemble the front panel interface board to the front panel assembly.

Table 10: Routine SA3D Signatures 1

SIGNAL	SIGNATURE	TEST POINT (IC PIN No.)							
		ML13 to ML21	ML12	ML9	ML8	ML25	ML6	ML4	ML26
DB0	UUOF	5	9	5	5	9	9	9	3
DB1	HP49	3	11	3	3	11	11	11	4
DB2	5319	2	13	2	2	13	13	13	6
DB3	9UPP	4	15	4	4	15	15	15	11

Table 11: Routine SA3D Signatures 2

SIGNAL	SIGNATURE	TEST POINT (IC PIN No.)					
		ML2	ML3	ML5	ML24	ML7	ML26
DB4	C646	9	9	9	-	9	13
DB5	HA85	11	11	11	-	11	14
DB6	6U62	13	13	13	13	13	-
DB7	UOUA	15	15	15	15	15	-

Table 12: Routine SA3D Signatures 3

SIGNAL	SIGNATURE	ML10	SIGNAL	SIGNATURE	ML10
S0	5290	11	S11	F8P8	19
S1	4095	9	S12	381F	14
S2	C304	10	S13	3F33	13
S3	930C	8	S14	8363	16
S4	53H9	7	S15	013C	15
S5	9725	6	N0	93H2	2
S6	H599	5	N1	9H03	3
S7	485H	4	N2	U891	21
S8	7CH4	18	N3	24H7	22
S9	H097	17	STROBE	8U40	23
S10	8P3H	20			

Routine SA3E - Modulation Board

46. (1) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	OUT (positive edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(2) Set the MA1723 POWER switch to OFF.

(3) Connect the signature analyser leads as follows:

START	ML5 pin 12, Front	
STOP	panel interface board	
CLOCK	TP1	Processor
GROUND	Lower end of R2	board

(4) Ensure that:

(a) Switches SB and SF on the processor board are both set to the closed (UP) position.

(b) Switches SA, SC, SD and SE on the processor board are set to the open (down) position.

(c) The AGC switches SA and SB on the modulation board are both set to the open (OFF) position i.e. towards the board edge.

(d) The LINE/SET/RF switch is set to the SET position.

(e) The VOX/PTT/TX switch is set to the PTT position.

(5) Set the MA1723 POWER switch to ON.

(6) Connect the signature analyser probe, in turn, to the following points on the modulation boad and check that correct signatures are obtained.

+5V	- ML26 pin 1	-	8U93
0V	- ML26 pin 8	-	0000

(7) Connect the signature analyser probe, in turn, to the points given in Tables 13, 14, 15 and 16, and check that correct signatures are obtained. As an aid to locating a device which is causing incorrect signatures on the modulation board data bus D0 to D7, any of the latches ML19, ML20, ML21, ML22 or ML29 may be removed without affecting the correct bus signatures.

Table 13: Routine SA3E Signatures 1

SIGNAL	SIGNATURE	TEST POINT (IC PIN No.)						
		ML19	ML20	ML21	ML22	ML27	ML28	ML29
DB0	UUOF	-	-	-	-	-	10	-
DB1	HP49	-	-	-	-	-	3	-
DB2	5319	-	-	-	-	-	6	-
DB3	9UPP	-	-	-	-	-	14	-
DB4	C646	-	-	-	-	6	-	-
DB5	HA85	-	-	-	-	3	-	-
DB6	6U62	-	-	-	-	10	-	-
DB7	UOUA	-	-	-	-	14	-	-
D0	UUOF	-	-	4	4	-	-	-
D1	HP49	-	-	7	7	-	-	-
D2	5319	-	-	13	13	-	-	-
D3	9UPP	-	-	14	14	-	-	-
D4	C646	14	4	-	-	-	-	4
D5	HA85	13	7	-	-	-	-	7
D6	6U62	7	13	-	-	-	-	13
D7	UOUA	4	14	-	-	-	-	14

Table 14: Routine SA3E Signatures 2

SIGNAL	SIGNATURE	TEST POINT (IC PIN No.)					
		ML12	ML16	ML22	ML29	ML31	ML32
B0	0A77	-	-	2	-	-	-
B2	2962	-	-	11	-	-	2
B3	P713	-	-	1	-	-	6,7
B4	0AH4	-	-	-	2	5	-
B5	89H0	12	-	-	10	-	-
B6	8HU7	6	-	-	11	-	-
B7	6127	-	12,6	-	1	-	-
CARRIER	2336	13,5	-	-	-	-	3

Table 15: Routine SA3E Signatures 3

SIGNAL	SIGNATURE	TEST POINT (IC PIN No.)						
		ML2	ML5	ML7	ML16	ML20	ML21	ML30
LSB+AGC	6668	-	-	6	-	10	-	9
LSB-AGC	644U	-	-	12	-	2	-	8
USB+AGC	892C	5	-	-	-	-	1	13
USB-AGC	3AF0	13	-	-	-	-	11	12
A	09UP	-	10	-	-	-	2	-
B	8U3P	-	9	-	-	-	10	-
2A6	C953	6	-	13	13	11	-	-
2A7	C98H	12	-	5	5	1	-	-

Table 16: Routine SA3E Signatures 4

SIGNAL	SIGNATURE	TEST POINT (IC PIN No.)						
		ML19	ML20	ML21	ML22	ML24	ML26	ML29
OP2A	F55C	-	-	-	-	-	14	-
OP2B	4716	-	-	-	-	-	3	-
OP2C	32C1	-	-	-	-	-	6	-
OP2A	F55C	-	5	5	-	-	13	-
OP2B	4716	-	-	-	5	-	4	5
OP2C	32C1	5	-	-	-	-	5	-
C	F9UU	2	-	-	-	9	-	-
B	UF48	10	-	-	-	10	-	-
A	U344	11	-	-	-	11	-	-

(8) Set the MA1723 POWER switch to OFF.

(9) Replace the front panel assembly.

Routine SA3F - Synthesizer Board Input Data

47. (1) Stand the unit so that it rests on the left-hand side member.

(2) Remove the push-fit screening cover from the synthesizer board compartment.

(3) Remove the six-side screening plate from the synthesizer board, secured with four captive screws.

(4) Follow the procedures given in paras. 46(1) to 46(4).

(5) Set the MA1723 POWER switch to ON.

(6) Connect the signature analyser probe, in turn, to the following points on the synthesizer board, and check that correct signatures are obtained.

+5V - ML12 pin 39 - 8U93
0V - ML12 pin 24 - 0000

(7) Connect the signature analyser probe, in turn, to the points given in table 17 and check that correct signatures are obtained.

Table 17: Routine SA3F Signatures

SIGNAL	SIGNA-TURE	ML12 PIN
DB0	UU0F	22
DB1	HP49	21
DB2	5319	20
DB3	9UPP	19
DB4	C646	18
OP29	P03H	17

(8) Set the MA1723 POWER switch to OFF.

(9) Disconnect all test equipment and replace all removed items (except the screening cover and plate from the synthesizer board if proceeding with self-test routine 21 - para. 48).

(10) Set switches SA to SF on the processor board to the open (down) position.

(11) Set the AGC switches SA and SB on the modulation board as required (the OFF position is towards the board edge).

Self-Test Routine 21

48. Self-test routine number 21 is a signature analysis routine for the synthesizer board. Due to the waveshape of the signal at TP8 on the synthesizer board, one of four possible sets of valid signatures may be obtained at the points given, and hence four sets of signatures are listed (in table 18). The procedure is as follows:

49. (1) Set the MA1723 POWER switch to OFF.

(2) Stand the unit so that it rests on the left-hand side member.

(3) Remove the push-fit screening cover from the synthesizer board compartment.

(4) Remove the six-sided screening plate from the synthesizer board, secured with four captive screws.

(5) Ensure that switches SA to SF on the processor board are all set to the open (down) position.

(6) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	IN (negative edge)
CLOCK pushbutton	IN (negative edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(7) Connect the signature analyser leads to the following test points on the synthesizer board:

START	TP8
STOP	TP8
CLOCK	TP6
GROUND	TP3

(8) Set the MA1723 POWER switch to ON.

(9) Press and hold the REM pushbutton, press and release the numeral 2 pushbutton followed by the numeral 1 pushbutton, and then release the REM pushbutton.

(10) Check that the MA1723 front panel displays are blanked apart from a flashing test number 21.

(11) Press and release the ENTER pushbutton to start the routine.

(12) Connect the signature analyser probe, in turn, to the following points on the synthesizer board and check that correct signatures are obtained.

+5V - ML12 pin 39 - 21F5
0V - ML12 pin 24 - 0000

(13) Connect the signature analyser probe, in turn, to the points given in table 18 and check that correct signatures (either A, B, C or D) are obtained.

(14) Switch off and disconnect all test equipment.

(15) Replace all removed items.

Table 18: Self-test Routine 21 Signatures

SIGNAL	SIGNATURE				TEST POINT (IC PIN No.)			
	A	B	C	D	ML12	ML18	ML11	ML19
DIV 1	51P4	825H	6U49	94AU	13	3	-	-
DIV 2	2H7P	9081	29AA	A246	12	4	-	-
DIV 3	0FCC	C144	086U	8383	11	5	-	-
DIV 4	0000	0000	0000	0000	10	6	-	-
DIV 5	21F5	21F5	21F5	21F5	9	-	3	-
DIV 6	21F5	21F5	21F5	21F5	8	-	4	-
DIV 7	21F5	21F5	21F5	21F5	7	-	5	-
DIV 8	0000	0000	0000	0000	6	-	6	-
DAC 1	028A	8P55	4PP9	4F45	33	-	-	5
DAC 2	9845	C919	9A77	664A	32	-	-	6
DAC 3	U2HU	A47P	46FC	C9U3	31	-	-	7
DAC 4	3508	A038	82A7	F56A	30	-	-	8
DAC 5	9FOH	3POF	1A29	0A7H	29	-	-	9
DAC 6	0UA8	62C0	15A3	4717	28	-	-	10
DAC 7	6600	6478	FU81	8044	27	-	-	11
DAC 8	4F9A	6H5U	825C	A39P	26	-	-	12

CHAPTER 21

PARTS LIST

CONTENTS

NOTES

This chapter gives parts list information for assemblies and chassis mounted components only. Detailed components lists for the printed circuit boards and modules are given at the end of the respective chapters.

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number

CHASSIS ASSEMBLY (ST82642)

Sub-Assemblies

		Power Supply Module			ST80548
		Synthesizer Board			ST81645
		Reference Generator Board			ST81647
		Modulation Board			ST81649
		Mixer Board			ST81651
		RF Output Board			ST81653
		Rear Panel Board			ST81655
		Processor Board			ST86051
		Front Sub-Panel Assembly			ST81935

Connectors

SK3/SK28		Cable assembly			BA82511/1
		Comprising:			
		Socket, coaxial (SK3)			916506
		Socket, coaxial (SK28)			916506
		Cable, coaxial, URM110			925438
SK2/SK23		Cable assembly			BA82511/1
		Comprising:			
		Socket, coaxial (SK2)			916506
		Socket, coaxial (SK23)			916506
		Cable, coaxial, URM110			925438
SK14/SK17		Cable assembly			BA82512/1
		Comprising:			
		Socket, coaxial (SK14)			938423
		Socket, coaxial (SK17)			938423
		Cable, coaxial, URM110			925438
SK15/SK26		Cable assembly			BA82512/2
		Comprising:			
		Socket, coaxial (SK15)			938423
		Socket, coaxial (SK26)			938423
		Cable, coaxial, URM110			925438
SK18/SK29		Cable assembly			BA82512/3
		Comprising:			
		Socket, coaxial (SK18)			938423
		Socket, coaxial (SK29)			938423
		Cable, coaxial, URM110			925438
SK19/SK33		Cable assembly			BA82512/4
		Comprising:			
		Socket, coaxial (SK19)			938423
		Socket, coaxial (SK33)			938423
		Cable, coaxial, URM110			925438

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Connectors (cont'd)					
SK20/SK22		Cable assembly			BA82512/5
		Comprising:			
		Socket, coaxial (SK20)			938423
		Socket, coaxial (SK22)			938423
		Cable, coaxial, URM110			925438
SK24/SK47		Cable assembly			BA82512/6
		Comprising:			
		Socket, coaxial (SK24)			938423
		Socket, coaxial (SK47)			938423
		Cable, coaxial, URM110			925438
SK30/SK32		Cable assembly			BA82512/8
		Comprising:			
		Socket, coaxial (SK30)			938423
		Socket, coaxial (SK32)			938423
		Cable, coaxial, URM110			925438
SK37/SK43		Cable assembly			BA82568/1
		Comprising:			
		Socket, 34-way (SK37)			934821
		Socket, 34-way (SK43)			934821
		Cable, flat, 34-way			931531
		Clamp, Strain Relief			934811
SK13/SK36		Cable assembly			BA82569/1
		Comprising:			
		Socket, 10-way (SK13)			934816
		Socket, 10-way (SK36)			934816
		Cable, flat, 10-way			931526
		Clamp, Strain Relief			934807
SK10/SK16/ SK21/SK34/ SK42		Cable assembly			BA82570
		Comprising:			
		Socket, 26-way (SK10)			934820
		Socket, 10-way (SK16)			934816
		Socket, 10-way (SK21)			934816
		Socket, 3-way (SK34)			938657
		Socket, 26-way (SK42)			934820
		Cable, flat, 26-way			939395
Rear Panel Mating Connectors					
		Socket, 3-way (PL1)			930766
		Plug, coaxial (SK2, SK3)			900038
		Plug, 25-way (SK4)			916489
		Shell, junction, 25-way			918108
		Retainer, 25-way			914245
		Plug, 37-way (SK5)			916507
		Shell, junction, 37-way			918106
		Retainer, 37-way			914246

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Potentiometers					
R1	10k	Resistor, Variable, Log			921011
R2	10k	Resistor, Variable, Log			921011
		Locking Cover			906368
Miscellaneous					
		Cover 1, Mixer Board			CD81748
		Cover 2, Mixer Board			CD82611
		Cover, Synthesizer Board			CD81749
		Cover, Reference Generator Board			CD81909
		Cover Plate assembly			BA82538
		Cover Box assembly			CA82539
		FRONT SUB-PANEL ASSEMBLY (ST81935)			
Sub-Assemblies					
		Front Panel Interface Board			ST81617
		Front Panel Display Board			ST81643
Connectors					
SK7/SK48		Cable assembly			BA82511/3
		Comprising:			
		Socket, coaxial (SK7)			916506
		Socket, coaxial (SK48)			938423
		Cable, coaxial, URM110			925438
PL11		Plug, 5-way			928268
SK8		LINE 1 Jack, 4-way			939955
SK9		LINE 2 Jack, 4-way			939955
SK44		Socket housing, 13-way			940043
		Pins, Crimp (SK44)			933111
Switches					
SA		POWER ON/OFF, toggle			939953
SB		LINE/SET/RF, toggle			939954
SC		VOX/PTT/TX, toggle			939954
		OPTIONAL ASSEMBLIES			
		Frequency Standard Kit S2			ST82650
		Consisting of:			
		Frequency Standard Assembly (9442)			ST82851
SK27/SK35		Cable assembly			BA82512/7
		Comprising:			
		Socket, coaxial (SK27)			938423
		Socket, coaxial (SK35)			938423
		Cable, coaxial, URM110			925438

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
		Frequency Standard Kit S3			ST82651
		Consisting of:			
		Frequency Standard Assembly (9420)			ST82852
SK27/SK35		Cable assembly			BA82512/7
		Comprising:			
		Socket, coaxial (SK27)			938423
		Socket, coaxial (SK35)			938423
		Cable, coaxial, URM110			925438
		SCORE Remote Control Kit			ST82458
		Consisting of:			
		SCORE Interface Board			ST81657
SK40/SK45		Cable assembly			BA82567/1
		Comprising:			
		Socket, 34-way (SK40)			934821
		Socket, 34-way (SK45)			934821
		Cable, flat, 34-way			931531
		Clamp, Strain Relief			934812
		FSK Kit			ST82542
		Consisting of:			
		FSK Board			ST82356
		Mounting hardware			

CHAPTER 22

EXTENDED CHANNEL INTERFACE BOARD

CONTENTS

Illustrations

Appendices

CHAPTER 22

EXTENDED CHANNEL INTERFACE BOARD

INTRODUCTION

1. The Extended Channel Interface Board is an optional internally-fitted board which provides for extended control of the drive unit. The board interfaces a channelised control unit, such as the LA1518 or MA1100, with the drive unit.

2. The board is located on the chassis as shown in Fig. 1.3 (annotated Optional Remote Interface Board). Interconnections are shown in Fig. 17.2 (the board is annotated Remote Interface Board (Option)). The board is interconnected by two cables, one connected to the rear panel via SK38, and one connected to the Processor Board via PL45.

3. The Extended Channel Interface Board physically replaces the Score Interface Board, an optional board used when the Racal SCORE system is fitted (ref. Chapter 14).

PRINCIPLES OF OPERATION

4. The MA1723 equipped with the Extended Channel Interface Board interfaces directly with the LA1518 HF Transmitter Control Decoder giving remote control of ten channels and associated transmitter functions. Alternatively it interfaces with the MA1100 Operator Terminal Unit giving extended control of 100 channels and associated transmitter functions. With either of these systems any of the auto-tuning Racal amplifiers may be used (TTA1885, TTA1860, TA1800) and in addition, with the ten channel system, the TA1820 channelised amplifier is suitable.

FACILITIES PROVIDED

5. The Extended Channel Interface Board accepts twelve control inputs and provides twelve revertive outputs all using Racal standard logic levels (see Appendix 1). The inputs and outputs are all available on rear panel socket SK5. The facilities provided are as follows.

Control Lines

6. Control lines are inputs to the software via the Interface Board, and are used to select the required parameters.

Channel Select

7. Two sets of four parallel lines, BCD coded. The BCD code entered on these lines selects a channel number at the MA1723 following a Load channel and Reset pulse.

Load Channel

8. When this line is set to '0' the channel number on the channel select lines is loaded into a buffer in the MA1723. The MA1723 continues to operate on the oroginal frequency.

9. Before loading the channel number a software check is carried out to ascertain that the channel select lines are within the limits 00-99. The channel select lines may change at any time but only the entries on the select lines when the LOAD channel is set to 0 V are accepted.

10. The load channel line may be changed several times while entering a number of valid channels, each time overwriting the last entry. If the load channel line is held permanently low the buffer is continuously updated with the channel number on the channel select lines.

Reset

11. When this line is at '0' the channel number in the buffer is used to select channel information from the stored channel and set the MA1723 to this channel. A reset cycle is then started which will tune up an amplifier.

12. Before tuning the channel information is recalled from memory, and a check is made on its validity (by a checksum).

13. If a channel without information is selected the reset does not allow a tune up cycle to commence.

14. The procedure to enter a new channel and retune the amplifier is as follows. Set up the channel select lines, take the Load channel line 'low', and then the Reset line 'low'. If the Load channel line and Reset line are both held at zero volts the MA1723 will automatically change channel and cause the amplifier to return whenever the number on the channel select line changes.

Off/Standby/EHT/Low Power

15. These two lines allow selection of the standby and EHT ON conditions of the associated linear amplifier and also to select low power output from the MA1723. The appropriate logic codes to select these functions are as follows:-

TABLE 1

SK5 PIN 7	SK5 PIN 6	FUNCTION
O/C	O/C	OFF
O/C	OV	STBY
OV	OV	EHT/STBY
OV	O/C	LOW POWER/EHT/STBY

'1' = Pulled-up to +12 V by internal resistor

REVERTIVE LINES

16. Revertive lines are outputs from the software, via the Interface Board and indicate conditions selected at the Drive Unit.

Revertive Channel Lines

17. Two sets of four parallel BCD coded lines for units and 10's channel revertive number. The revertive channel number is available in both local and remote conditions. If a channel number is not shown on the MA1723 the output is FF (hexadecimal).

Remote On

18. This line is at 0 V if the MA1723 is in Remote control.

Transmit

19. This line is at 0 V if the MA1723 is in the TUNE or Transmit condition.

Fault

20. This line is at 0 V if the MA1723 has an internal fault or if an external fault is signalled by the amplifier.

Revertive Reset

21. This line is at 0 V if:

(1) A new channel number has been set up and a load channel pulse has been sent to the MA1723. The next reset pulse input causes the MA1723 to operate on the new channel, the amplifier to return and sets the revertive reset line to open circuit.

(2) The Reset LED on the MA1723 front panel is illuminated. The Reset LED is illuminated when a fault occurs, Standby is selected or at switch on. The next reset pulse extinguishes the Reset LED, retunes the amplifier and sets the revertive reset line to open circuit.

(3) No Ready signal is produced by the amplifier.

REAR PANEL CONNECTIONS

22. Socket SK38 of the Interface Board is connected to the Rear Panel Board (Fig. 17.2) and then to socket SK5 on the rear panel (Fig. 12.1). The facilities available at this socket are as follows:

SK5 PIN

1	0 V
2	FAULT
3	REMOTE ON
4	LOAD CHANNEL
5	RESET
6	STBY
7	EHT

See Table 1

8	0 V
9	2^3 UNITS CHANNEL NO. SELECT
10	0 V
11	2^2 UNITS CHANNEL NO. SELECT
12	0 V
13	2^1 UNITS CHANNEL NO. SELECT
14	0 V
15	2^0 UNITS CHANNEL NO. SELECT
16	0 V
17	2^3 TENS CHANNEL NO. SELECT
18	0 V
19	0 V
20	0 V
21	TRANSMIT
22	REVERTIVE RESET
23	0 V
24	2^0 TENS CHANNEL NO. SELECT
25	2^1 TENS CHANNEL NO. REVERTIVE
26	2^2 TENS CHANNEL NO. REVERTIVE
27	2^3 TENS CHANNEL NO. REVERTIVE
28	No connection
29	2^0 UNITS CHANNEL NO. REVERTIVE
30	2^1 UNITS CHANNEL NO. REVERTIVE
31	2^2 UNITS CHANNEL NO. REVERTIVE
32	2^3 UNITS CHANNEL NO. REVERTIVE
33	2^0 TENS CHANNEL NO. REVERTIVE
34	0 V
35	2^1 TENS CHANNEL NO. SELECT
36	0 V
37	2^2 TENS CHANNEL NO. SELECT

OFF/STANDBY/EHT/LOW POWER FUNCTIONS

23. These functions are selected by various logic combinations which are fed in via SK5 pins 6 and 7.

CIRCUIT DESCRIPTION (Fig. 1)

24. Channel selection inputs, in BCD, are fed to pins 12, 4, 2, 3 of SK38 (ones input) and to pins 30, 6, 8, 10 of SK38 (tens input). These inputs are normally held at logic '1' by the resistor package R1, and are pulled to 0 V by active low inputs.

25. Integrated circuit ML11b is a decoder whose outputs are determined by the PA0, PA1, PA6 and strobe inputs from the Processor Board. When the Strobe and PA6 inputs are both at '1' the gate ML14b provides a '0' $\overline{\text{ENABLE}}$ input to ML11b (pin 15) allowing ML11b to provide binary logic outputs at Q0, Q1 and Q2 (pins 12, 11, 10), in accordance with the A and B inputs at pins 14 and 13.

26. ML7a and ML7b are level changes converting the +5 V input levels from ML11b to the +12 V levels required by CMOS gates ML4a, b, ML5a, b, ML8a, b and ML9a, b. When ML7a (pin 4) is at '1' the units channel select inputs (from SK38) are fed, in inverted form, to the data bus DB0 to DB3. Similarly, when ML7b (pin 5) is at '1' the tens channel select inputs (from SK38) are fed, in inverted form, to the data bus DB0 to DB3.

27. A load channel '0' input (SK38 pin 11) is converted to '1' by ML6a (pulled up to +5 V by R8) and used to set the D-type flip-flop ML13a, giving a '0' at $\overline{Q}$ (pin 2) which is inverted to '1' by ML12a when a strobe pulse is received from ML11b Q2 output (para. 25). The pulse is then fed to data bus DB4.

28. A reset '0' input, at SK38 pin 9, is fed to the bus in a similar manner to the load channel input. Gates ML6b, ML12b and flip-flop ML13b are used.

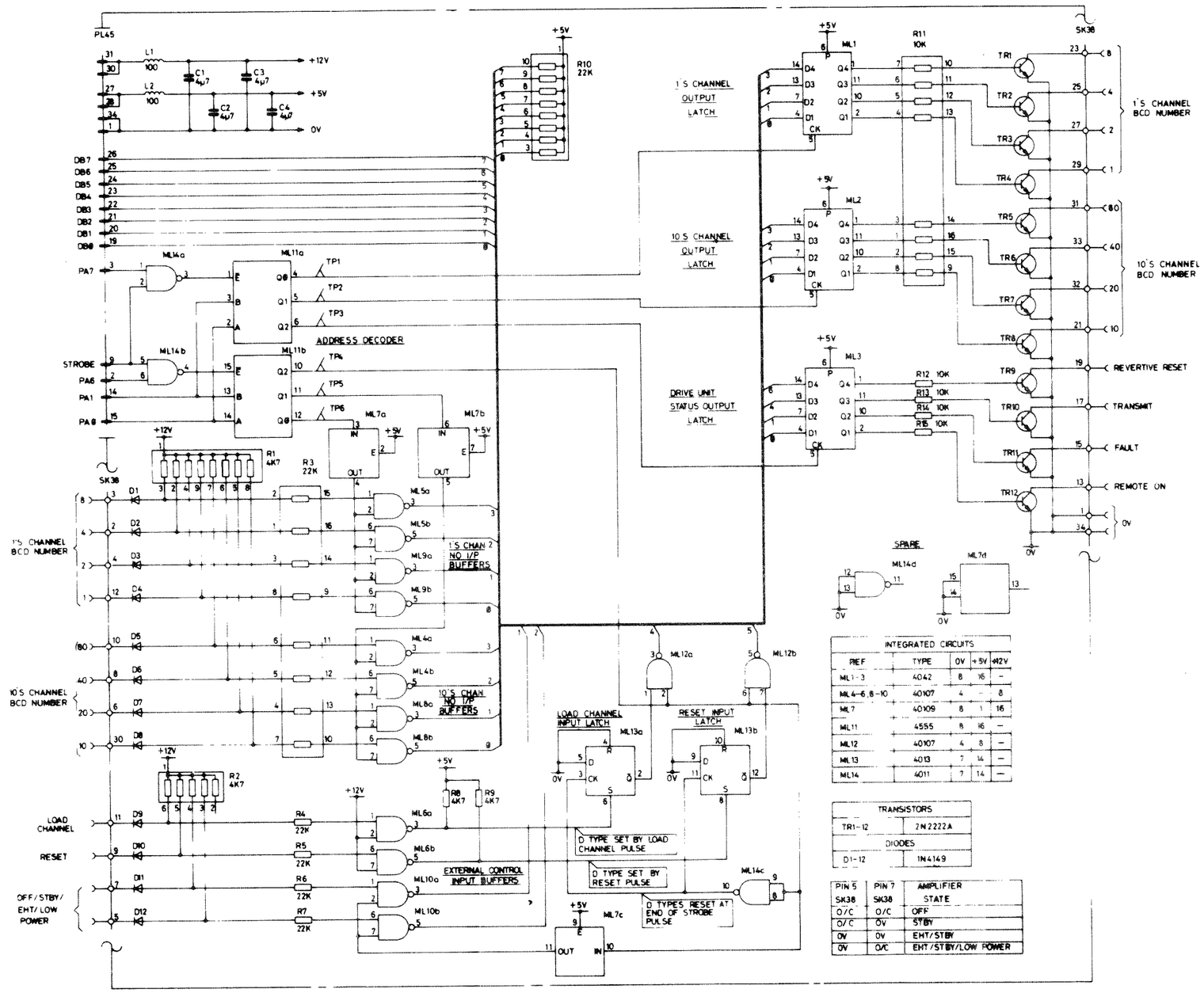
29. Gates ML10a and ML10b act as inverters when a strobe pulse from ML11b Q2 is applied (via level charger ML7c). This allows the OFF/STANDBY/EHT/LOW POWER select inputs (SK38 pins 7 and 5) to be fed to the DB1 and DB2 data bus lines.

30. The strobe pulse from ML11b Q2 output is inverted by ML14c and applied to the CLOCK inputs of ML13a (pin 3) and ML13b (pin 11). The effect of this is to clock the '0' at the D inputs into the flip-flops at the end of the strobe pulse producing a '1' at the $\overline{Q}$ outputs. Thus the flip-flops are ready to be set by further load channel and reset pulses as described in paras. 27 and 28.

31. ML11a is used to clock the latches ML1, ML2, ML3 (in a similar manner to ML11b, para. 25) when STROBE and PA7 inputs are both at '1' and are applied to ML14a, giving a '0' $\overline{\text{ENABLE}}$ to ML11a. The latches provide revertive outputs from the data bus at the Q1 to Q4 output of each latch. Transistors TR1 to TR12 are drivers for the revertive outputs.

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
		EXTENDED CHANNEL INTERFACE BOARD			
		ST 82449			
Resistors					
R1	4k7	Resistor Network			939133
R2	4k7	Resistor Network			939133
R3	22k	Resistor Network			936375
R4	22k	Metal Oxide		2	913493
R5	22k	Metal Oxide		2	913493
R6	22k	Metal Oxide		2	913493
R7	22k	Metal Oxide		2	913493
R8	4k7	Metal Oxide		2	913490
R9	4k7	Metal Oxide		2	913490
R10	22k	Resistor Network			935012
R11	10k	Resistor Network			936374
R12	10k	Metal Oxide		2	914042
R13	10k	Metal Oxide		2	914042
R14	10k	Metal Oxide		2	914042
R15	10k	Metal Oxide		2	914042
Capacitors			V		
C1	4µ7	Tantalum	35	20	914026
C2	4µ7	Tantalum	35	20	914026
C3	4µ7	Tantalum	35	20	914026
C4	4µ7	Tantalum	35	20	914026
Diodes					
D1		1N4149			914898
D2		1N4149			914898
D3		1N4149			914898
D4		1N4149			914898
D5		1N4149			914898
D6		1N4149			914898
D7		1N4149			914898
D8		1N4149			914898
D9		1N4149			914898
D10		1N4149			914898
D11		1N4149			914898
D12		1N4149			914898

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Transistors					
TR1		2N2222A			923217
TR2		2N2222A			923217
TR3		2N2222A			923217
TR4		2N2222A			923217
TR5		2N2222A			923217
TR6		2N2222A			923217
TR7		2N2222A			923217
TR8		2N2222A			923217
TR9		2N2222A			923217
TR10		2N2222A			923217
TR11		2N2222A			923217
TR12		2N2222A			923217
Integrated Circuits					
ML1		CD4042			930861
ML2		CD4042			930861
ML3		CD4042			930861
ML4		CD40107			931052
ML5		CD40107			931052
ML6		CD40107			931052
ML7		CD40109			931054
ML8		CD40107			931052
ML9		CD40107			931052
ML10		CD40107			931052
ML11		CD4555			928189
ML12		CD40107			931052
ML13		CD4013			926860
ML14		CD4011			930028
Miscellaneous					
SK38		Plug, 34-way			940000
PL45		Plug, 34-way			939991
L1		Inductor, 100 µH	0.2	10	939161
L2		Inductor, 100 µH	0.2	10	939161



INTEGRATED CIRCUITS				
REF	TYPE	0V	+5V	+12V
ML1-3	4042	8	16	–
ML4-6, 8-10	40107	4	–	8
ML7	40109	8	1	16
ML11	4555	8	16	–
ML12	40107	4	8	–
ML13	4013	7	14	–
ML14	4011	7	14	–

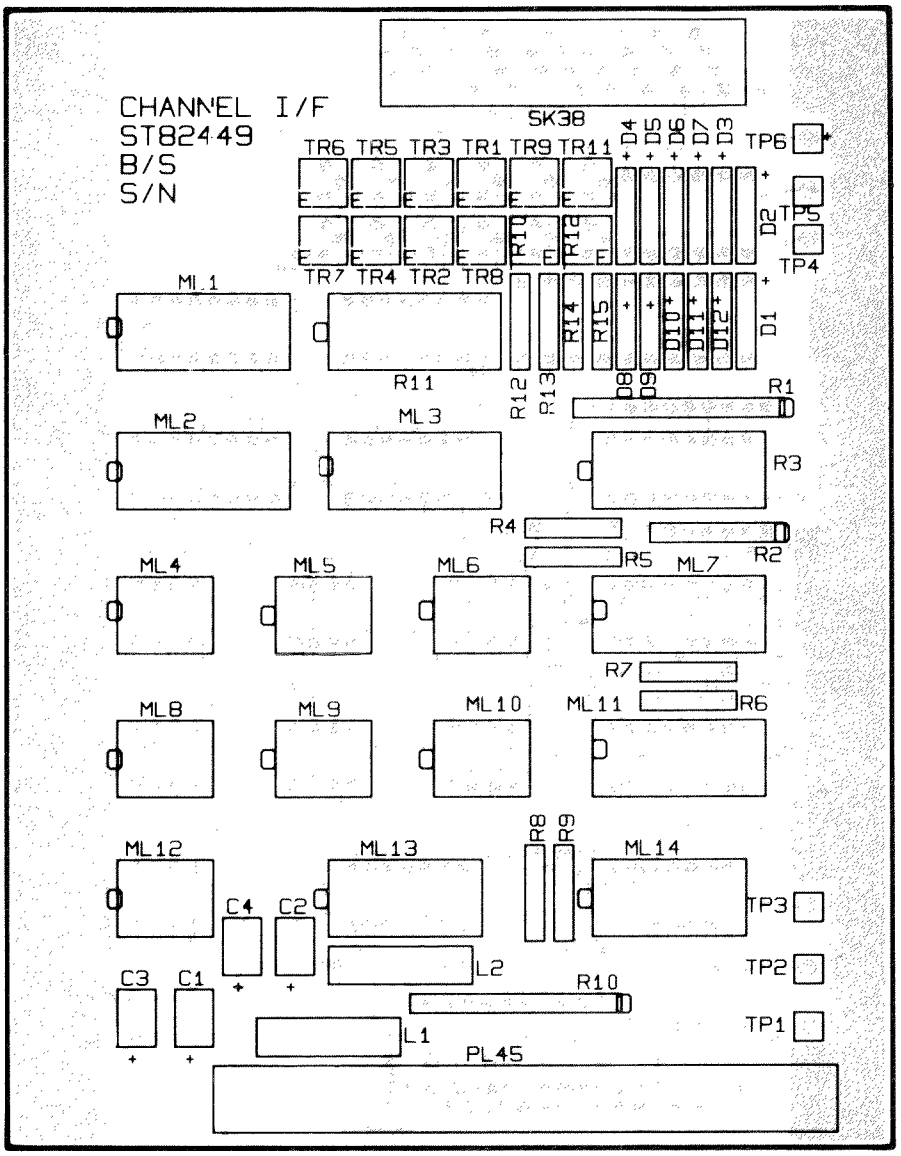
TRANSISTORS	
TR1-12	2N2222A
DIODES	
D1-12	1N4149

PIN 5 SK38	PIN 7 SK38	AMPLIFIER STATE
O/C	O/C	OFF
O/C	0V	STBY
0V	0V	EHT/STBY
0V	O/C	EHT/STBY/LOW POWER

RACAL

TH 3071	DC 82449	22.1
1		

Circuit:
Extended Channel Interface Board. Fig. 22.1



Layout :
Extended Channel Interface Board

Fig.22.2

RACAL
DA02448

APPENDIX 1

RACAL STANDARD INTERFACE LOGIC

Racal standard interface logic levels conform to the following parameters:

Logic Inputs: ON State (Short Circuit to 0 volt)

Steady state short circuit current to 0 volt shall be less than 40 milliamps. (Approximately 2.5mA in the MA1723).

OFF State (Open Circuit)

Internally pulled up to a voltage between +5 volts and +28 volts (+12 V in the MA1723). The voltage at this terminal, including transients at no time exceeds +30 volts.

Logic Outputs: ON State (Short Circuit to 0 volt)

Output Voltage:

0 to 0.5 volt for current less than 10 milliamps.

0 to 1.0 volt for current from 10 milliamps to 50 milliamps.

OFF State (Open Circuit)

Leakage current less than 10 microamps for voltages up to 30 volts.

RACAL COMMUNICATIONS LTD

Amendment to

MA 1723 HF DRIVE UNIT

C/R 73736

Page 19-25

Para 27(5) After Vertical Scale
Add Input Attenuator - 10 dB

Page 19-26

Para 28(8) After Vertical Scale
Add Input Attenuator - 0 dB

RACAL COMMUNICATIONS LIMITED

Amendment to

MA 1723 HF DRIVE UNIT

CR 73923

CHAPTER 20 Pages 20-11 to 20-33

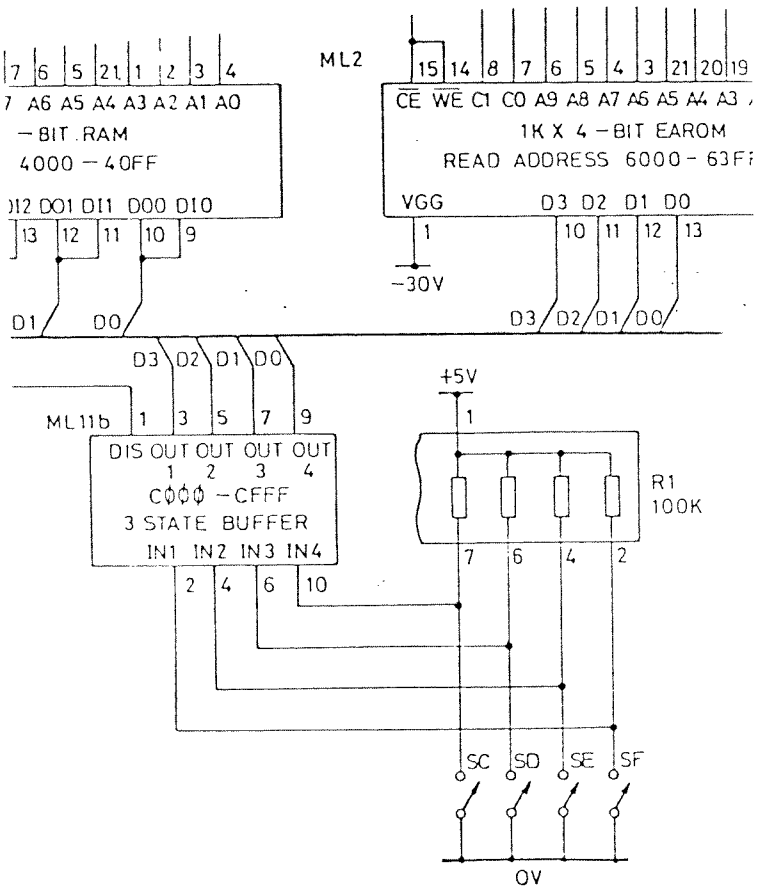
Remove and destroy old pages, insert new pages attached.

FIG. 6.1

Amend ML 11b to read CØØØ - CFFF

not 3ØØØ - 3FFF

as shown below



Signature Analysis Routines

30. Three of the four signature analysis routines, designated SA1, SA2 and SA3, are selected by first setting the front panel POWER switch to OFF, setting the processor board DIL switches SA to SF to the appropriate positions given below, and then returning the POWER switch to ON. The fourth signature analysis routine is included with the self-test routines, as number 21, and is described in para. 48.

Processor Board DIL Switch Settings

FUNCTION SELECTED	DIL SWITCH					
	A	B	C	D	E	F
NORMAL	0	0	0	0	0	0
SA1	C	0	0	0	0	0
SA2	0	C	0	0	0	0
SA3	0	C	0	0	0	C

0 denotes Open (Down)
C denotes Closed (Up)

Routine SA1

31. Closure of test switch SA on the processor card causes the CPU to continuously cycle through the entire address field and to read onto the data bus the data found at each addressed location. This routine is used to check the CPU device (ML1), and the connections between it and other devices on the processor board. The procedure is given in para. 38.

Routine SA2

32. This routine is used to test the RAM, PIO and clock/timer circuitry on the processor board. The procedures are given in para. 39.

Routine SA3

33. This multi-purpose routine is used to test various parts of the front panel display board, the front panel interface board, the modulation board and the synthesizer board. The procedures are given in paras. 40 to 47.

Use of Signature Analyser

34. The type of signature analyser required to carry out the procedures given in this chapter has an integral logic probe which may be used as a test instrument independently of the signature measuring capability. The logic probe incorporates a lamp, and this may be used to indicate one of the following four conditions:

(1) Probe lamp OFF (L) - Logic '0' (GND)

(2) Probe lamp ON (H) - Logic '1'

(3) Probe lamp half ON - High Impedance/poor logic level

(4) Probe lamp flashing (F) - Data stream

35. The signature analyser has START, STOP and CLOCK inputs for connection to the circuit under test, and a logic probe for connection to a circuit node to obtain a signature. The logic levels at the START, SOP and logic probe inputs are strobed into the signature analyser on either the rising or falling edge of the CLOCK input (as selected by the CLOCK pushbutton). Either rising or falling edges of the START and STOP inputs may be selected to initiate and terminate a time period (window or gate) during which measurement takes place.

36. When the START, STOP, CLOCK and GROUND connections are made correctly and the signature analysis routine is being executed, the GATE indicator should flash. The correct configuration for a particular test can be verified by checking the logic '1' signature, obtained by connecting the probe tip to the positive supply.

37. If the HOLD pushbutton is depressed, the instrument will hold a single one-time signature. The probe can then be removed from the test node whilst the signature comparison is made. The displayed signature is reset by pressing and releasing the RESET button on the probe.

Routine SA1 Procedures (Processor CPU and ROM)

38. (1) Set the front panel POWER switch to OFF.

(2) On the processor board, set switch SA to the closed (UP) position, and ensure that the remaining switches, SB to SF, are all in the open (down) position.

(3) Disconnect the socket mating with PL40 on the processor board (if fitted).

(4) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	IN (negative edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(5) Connect the signature analyser leads to the processor board as follows:

START	TP5
STOP	PIN 4 ML12
CLOCK	TP1
GROUND	Lower end of R2 (0V)

(6) Set the MA1723 POWER switch to ON, and then connect the signature analyser probe, in turn, to any convenient +5V pin (e.g. ML1 pin 40), and to 0V, and check that the following signatures are obtained.

+5V	5FU8
0V	0000

(7) Connect the signature analyser probe, in turn, to the points given in Tables 1 and 2, and check that correct signatures are obtained.

NOTE 1: The signatures on data bus lines D0 to D7 are dependent on the version and issue number of the program contained in ROM devices PD1 and PD2. The correct signatures may be obtained from a known working unit fitted with the same program.

NOTE 2: Incorrect signatures on the data bus lines D0 to DC7 could be due to a faulty integrated circuit device connected to the data bus. With the exception of ML1, PD1 and PD2, any other integrated circuit connected to the data bus may be removed without affectinng the correct bus signatures.

Routine SA2 Procedures (Processor RAM and PIO)

39. (1) Set the front panel POWER switch to OFF, disconnect SK40 from PL40 on the processor board, release the four captive screws securing the processor board, and lift the board out of the unit, to hinge on the ribbon cable SK39 to PL39 on the front panel interface board.

(2) On the processor board, set switch SB to the closed (UP) position, the remaining switches, SA and SC to SF, to the open (down) position.

(3) At the MA1723 front panel, set the LINE/SET/RF switch to SET, and set the VOX/PTT/TX switch to TX.

(4) Set the signature analyser controls as follows:

Table 1: Processor Input and Output Signatures

SIGNAL	TEST POINT	SIGNATURE	
VCC	ML1 pin: 16	5FU8	INPUTS
VDD	40	5FU8	
VSS	20	0000	
$\overline{\text{CLEAR}}$	3	5FU8	
$\overline{\text{WAIT}}$	2		
CLOCK	1	5FU8F	
$\overline{\text{DMA IN}}$	38	5FU8	
$\overline{\text{DMA OUT}}$	37	0000	
$\overline{\text{INT}}$	36	5FU8	
TPA	34	0000F	OUTPUTS
TPB	33	0000F	
SC0	6	0000	
SC1	5	5FU8	
$\overline{\text{MRD}}$	7	0000F	
$\overline{\text{MWR}}$	35	5FU8	

F denotes flashing probe

Table 2: Processor Board ROM and Timing Signatures

SIGNAL	SIGNATURE	TEST POINT (IC PIN No.)														
		ML1	ML7	ML8	ML11	ML12	ML13	ML14	PD1	PD2	ML17	ML9	ML4	ML5	ML2	ML3
A0	3457	25				0000			10	10						
A1	13FH	26				04HU			9	9						
A2	50F3	27					50F31		8	8						
A3	411H	28					411H2		7	7						
A4	7233	29				1180	72333		6	6						
A5	P37H	30				755U	P37H4		5	5						
A6	9FFA	31				0000(F)	9FFA16		4	4						
A7	14P7	32					14P715		3	3						
TPA	0000F	34		11			17				11	1				
$\overline{MRD}$	0000F	7	15					12	22	22		39	18	18		
$\overline{AV}$	0000F		6	2			5,6									
$\overline{MWR}$	5FU8	35						11					20	20		
0V	0000(F)	20	8	7	8	8	9	7	14	14	10	20	8	8		
+5V	5FU8	16,40	16	14	16	16	18	14	1,28	1,28	20	40	22	22		
A8	6510								25	25	19				5	5
A9	A623								24	24	18				6	6
A10	808P								21	21	17				7	7
A11	7097								23	23	16				8	8
A12	A82C								2	2	15					
A13	2964								26	26	14					
A14	64HU					2					13					
A15	1180					3					12					
Y0	755U					4			20							
Y2	4H78					6				20						
Y3	5FU8				1	7										
$\overline{XTAL}$	0000F	39														
D.CK	0000F		2	3												
$\overline{AR}$	0000F		5	4												
$\overline{MRD.MWR}$	0000		9					10								

START pushbutton	OUT (positive edge)
STOP pushbutton	IN (negative edge
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(5) Connect the signature analyser leads to the processor board as follows:

START	TP8
STOP	TP8
CLOCK	TP1
GROUND	Lower end of R2 (0V)

(6) Set the MA1723 POWER switch to ON, and then connect the signature analyser probe, in turn, to any convenient +5V pin (e.g. ML1 pin 40), and to 0V, and check that the following signatures are obtained:

+5V	9A1A
0V	0000

(7) Check that the RUN/FAULT LED D1 on the processor board is flashing dimly approximately at the rate of two flashes per second.

(8) Connect the signature analyser probe, in turn, to the test points given in Table 3 and check that correct signatures are obtained.

(9) Set the MA1723 POWER switch to OFF.

(10) At the signature analyser, set the START pushbutton to the IN (logic '0') position, and set the STOP pushbutton to the OUT (logic '1') position.

(11) Set the MA1723 POWER switch to ON, and then connect the signature analyser probe, in turn, to any convenient +5 V pin (e.g. ML1 pin 40), and to 0 V, and check that the following signatures are obtained:

+5 V	UU83
0 V	0000

(12) Connect the signature analyser probe, in turn, to the test points given in tables 4 and 5, and check that correct signatures are obtained.

(13) Set the MA1723 POWER switch to OFF, disconnect the signature analyser leads, and return the processor board to the unit.

Table 3: Processor Board RAM Signatures

SIGNAL	SIGNATURE	TEST POINT (IC PIN No.)						
		ML1	ML13	ML4	ML5	ML11	ML14	ML9
$\overline{EFI}$	0000	24	-	-	-	-	-	-
$\overline{CS3}$	9A1A	-	10	-	-	14	-	-
$\overline{CS2}$	9A1A	-	11	-	-	12	-	-
$\overline{CS0}$	H5P2	-	13	-	-	-	2	-
A0	62A1	-	-	4	4	-	-	-
A1	PP5H	-	-	3	3	-	-	-
A2	5U27	-	-	2	2	-	-	-
A3	2HFH	-	-	1	1	-	-	-
A4	3118	-	-	21	21	-	-	-
A5	FAFA	-	-	5	5	-	-	-
A6	1827	-	-	6	6	-	-	-
A7	CU3P	-	-	7	7	-	-	-
$\overline{CS1}$	H5P2	-	-	19	19	-	1	-
CS2	9A1A	3	-	17	17	-	13	13
$R/\overline{W}$	6FA0	35	-	20	20	-	11	-
OD	49UC	7	-	18	18	-	12	39
DO	0C4F	15	-	-	9,10	-	-	-
D1	3462	14	-	-	11,12	-	-	-
D2	A59A	13	-	-	13,14	-	-	-
D3	H701	12	-	-	15,16	-	-	-
D4	C747	11	-	9,10	-	-	-	-
D5	95U4	10	-	11,12	-	-	-	-
D6	5682	9	-	13,14	-	-	-	-
D7	74H1	8	-	15,16	-	-	-	-

Table 4: Processor Board PIO Signatures

SIGNAL	SIGNATURE	TEST POINT (COMPONENT PIN No.)				
		ML9	ML1	ML8	SK39	PL40
'B' STROBE	0000	17	-	-	-	-
'A' READY	0000F	36	-	9	-	-
$\overline{\text{CLEAR}}$	UU83	13	3	-	-	9
'A' STROBE	6FF4	35	-	13	-	-
D0	510U	5	15	-	-	-
D1	07PA	6	14	-	-	-
D2	71AA	7	13	-	-	-
D3	3CU7	8	12	-	-	-
D4	53A7	9	11	-	-	-
D5	88F0	10	10	-	-	-
D6	H223	11	9	-	-	-
D7	6PAU	12	8	-	-	-
$\overline{\text{STROBE}}$	9347	-	-	12	9	-
WR/$\overline{\text{RE}}$	0000F	38	33	10	-	-
RD/$\overline{\text{WE}}$	0FF8	39	7	-	-	-

Table 5: Procesor Board Clock/Timing Signatures

SIGNAL	SIGNATURE	TEST POINT (COMPONENT PIN No.)			
		ML1	ML6	ML9	ML8
CLOCK	0000F	33	10	37,38	10
$\overline{\text{RESET}}$	0000	-	11	-	-
$\overline{\text{INT}}$	UU83	36	-	-	-
$\overline{\text{EF4}}$	UU83	21	-	-	-
$\overline{\text{TPA}}$	0000F	34	-	1	11
$\overline{\text{MRD}}$	0FF8	7	-	39	-
$\overline{\text{CLEAR}}$	UU83	3	-	13	-
N0	9889	19	-	3	-
N1	4101	18	-	4	-
N2	4101	17	-	2	-

Routine SA3 Procedure (Multi-purpose)

40. Routine SA3 is divided into six parts as follows:

A - Port Address Line Decoding (Para. 42)
B - Output Port Strobe Lines and Data Bus (Para. 43)
C - Input Port Strobe Lines and Data Bus (Para. 44)
D - Display Board (Para. 45)
E - Modulation Board (Para. 46)
F - Synthesizer Board Input Data (Para. 47)

Preliminary

41. (1) Set the MA1723 POWER switch to OFF

(2) Set switches SB and SF on the processor board to the closed (UP) position, and set the remaining switches, SA, SC, SD and SE, to the open (down) position.

(3) Remove the four screws securing the front panel to the front panel assembly, two screws at each edge (not the two recessed screws), and remove the front panel.

(4) Remove the remaining two screws securing the front panel assembly to the unit. Gently ease the front panel assembly forward and lower to 'hinge' on the connecting cableforms.

NOTE: Support the edges of the lowered front panel assembly to prevent inadvertant operation of any of the front panel pushbutton switches.

(5) Disconnect the socket mating with PL40 on the processor board (if fitted).

(6) Disconnect the FSK board (if fitted) from PL46 on the rear panel board.

(7) On the modulation board, set the USB and LSB AGC switches SA and SB to the open (off) position.

(8) Ensure that no external connections are made to SK4 or SK6on the rear panel, and that no connections are made to the front panel LINE 1 and LINE 2 sockets.

(9) At the front panel, set the LINE/SET/RF switch to SET, and set the VOX/PTT/TX switch to PTT.

(10) Set the signature analyser controls as follows:

START pushbutton	OUT (positive edge)
STOP pushbutton	IN (negative edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(11) Connect the signature analyser leads as follows:

START	ML5 pin 12, front	
STOP	Panel interface board	
CLOCK	TP1	On the processor
GROUND	Lower end of R2	board

(12) Temporarily raise the front panel assembly, set the POWER switch to ON, and check that the front panel displays are as given in Fig. 20(a).

(13) Check that the STANDBY and EHT LED indicators are flashing rapidly.

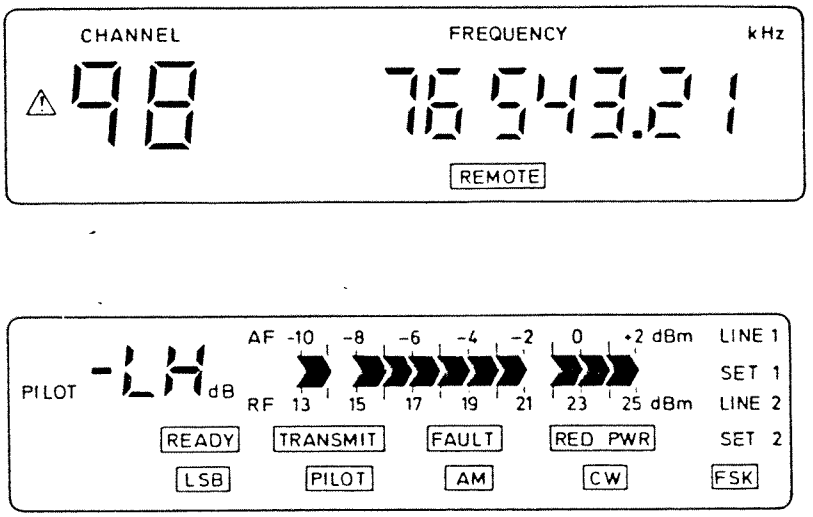


Fig. 20(a) Routine SA3 Front Panel Displays

(14) Connect the signature analyser probe in turn, to the following points on the front panel interface board and check that correct signatures are obtained.

+5V - Positive end of C1 - 82CP
0V - Negative end of C1 - 0000

Routine SA3A - Port Address Line Decoding

42. (1) Connect the signature analyser probe, in turn, to the points on the front panel interface board given in Table 6 and check that correct signatures are obtained.

Table 6: Routine SA3A Signatures

SIGNAL	SIGNATURE	TEST POINT (COMPONENT PIN No.)					
		PL39	ML6	ML9	ML5	ML1	TP1
PA0	6HU0	15	11	2	-	-	-
PA1	58H6	14	10	3	-	-	-
PA2	270U	13	9	21	-	-	-
PA3	0000F	12	-	22	-	-	-
PA4	82CPF	11	-	-	12	8	-
PA6	0000	5	-	-	2	-	-
PA7	0000	4	-	-	1	-	-
STROBE	4709	9	3	-	-	9,1	TP1
+5V	82CP	27	16	1	13	14	-
INHA	0000F	-	6	-	-	13,4	-
INHB	82CPF	-	-	23	-	-	-
ML5/3	0000	-	-	-	3	5	-
ML5/11	0000F	-	-	-	11	6	-
ML1/3	4497	-	-	-	-	3,12	-

Routine SA3B - Output Strobe Lines & Data Bus

43. (1) Set the signature analyser controls as follows:

START pushbutton	IN (logic '0')
STOP pushbutton	OUT (logic '1')
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(2) Set the MA1723 POWER switch to OFF.

(3) Connect the signature analyser leads as follows:

START)	ML5 pin 12,	
STOP)	Front panel interface board	
CLOCK	TP1	) Processor
GROUND	Lower end of R2	) Board

(4) Ensure that:

(a) Switches SB and SF on the processor board are both set to the closed (UP) position.

(b) Switches SA, SC, SD and SE on the processor board are set to the open (down) position.

(c) The AGC switches SA and SB on the modulation board are both set to the open (off) position.

(d) The LINE/SET/RF switch is set to the SET position.

(e) The VOX/PTT/TX switch is set to the PTT position.

(5) Set the MA1723 POWER switch to ON.

(6) Connect the signature analyser probe, in turn, to the points on the front panel interface board given below and check that correct signatures are obtained.

+5V - Positive end of C1 - 8U93
0V - Negative end of C1 - 0000

(7) Connect the signature analyser probe, in turn, to the points given in Tables 7 and 8, and check that correct signatures are obtained. Incorrect signatures on the DB0 to DB7 lines may be due to a faulty integrated circuit device connected to the data bus. As an aid to fault location, any integrated circuit device on the front panel interface board connected to the data bus may be removed without affecting the correct bus signatures. The front panel display board, modulation board and synthesizer board may also be disconnected.

Table 7: Routine SA3B Signatures 1

SIGNAL	SIGNATURE	TEST POINT (COMPONENT PIN No.)									
		ML10	ML3	ML14	ML8	ML7	SK31	SK25	SK12	PL39	PL41
DB0	UUOF	1	4	3	3	4	2	2	10	19	10
DB1	HP49	2	7	4	4	12	1	1	13	20	13
DB2	5319	3	13	6	6	13	3	3	14	21	14
DB3	9UPP	4	14	11	11	3	5	5	15	22	15
DB4	C646	5	-	13	13	-	6	-	11	23	11
DB5	HA85	6	-	14	14	-	-	-	12	24	12
DB6	6U62	7	-	-	-	-	-	-	17	25	17
DB7	UOUA	8	-	-	-	-	-	-	16	26	16
+5V	8U93	-	16	16	16	16	20	20	37	27	21
N0	93H2	-	-	-	-	6	-	-	-	-	
N1	9H03	-	-	-	-	11	-	-	-	-	
N2	U891	-	-	-	-	14	-	-	-	-	
N3	24H7	-	-	-	-	2	-	-	-	-	

Table 8: Routine SA3B Signatures 2

SIGNAL	SIGNATURE	TEST POINT (IC PIN No.)								
		ML3	ML4	ML5	ML7	ML8	ML9	ML10	ML11	ML14
TP11	00H3	-	-	8	-	-	11	-	-	-
TP13	8UUC	5	-	-	-	-	15	-	-	-
TP14	32C1	-	-	-	-	-	14	-	-	-
TP15	4716	-	-	-	-	-	19	-	-	-
TP16	F55C	-	-	-	-	-	20	-	-	-
TP17	P03H	-	-	-	-	-	17	-	-	-
TP18	9ACA	-	-	-	-	-	4	-	-	-
TP19	87C9	-	-	-	-	9	6	-	-	-
TP20	PCF1	-	-	-	-	-	7	-	-	9
TP21	A5P8	-	-	6	-	-	10	-	-	-
TP22	1208	-	-	-	1	-	9	-	-	-
+5V	8U93	6	1,15	5,9	10	1	24	-	-	16
$\overline{CE}$	2A7C	-	-	4	-	-	-	9	-	-
$\overline{CS}$	0000	-	-	-	-	-	-	10	-	-
+VCC	8U93	-	-	-	-	-	-	11	-	-
Q1	853P	2	3	-	-	-	-	-	-	-
Q2	4902	10	6	-	-	-	-	-	-	-
Q3	331C	11	10	-	-	-	-	-	-	-
Q4	F251	1	14	-	-	-	-	-	-	-
ST	8U40	-	-	10	15	-	-	-	-	-
A	853P	-	4	-	-	-	-	10	-	-
B	4902	-	5	-	-	-	-	11	-	-
C	331C	-	11	-	-	-	-	14	-	-
D	F251	-	13	-	-	-	-	13	-	-

Routine SA3C - Input Port Strobe Lines and Data Bus

44. (1) Set the signature analyser controls as follows:

START pushbutton	OUT (positive edge)
STOP pushbutton	IN (negative edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(2) Set the MA1723 POWER switch to OFF.

(3) Connect the signature analyser leads as follows:

START)	ML5 pin 12, Front
STOP)	panel interface board
CLOCK	TP1) Processor
GROUND	Lower end of R2) board

(4) Ensure that:

(a) Switches SB and SF on the processor board are both set to the closed (UP) position.

(b) Switches SA, SC, SD and SE on the processor board are set to the open (down) position.

(c) The AGC switches SA and SB on the modulation board are both set to the open (OFF) position.

(d) The LINE/SET/RF switch is set to the SET position.

(e) The VOX/PTT/TX switch is set to the PTT position.

(5) Set the MA1723 POWER switch to ON.

(6) Connect the signature analyser probe, in turn, to the points on the front panel interface board given below and check that correct signatures are obtained:

+5V - Positive end of C1 - 82CP
0V - Negative end of C1 - 0000

(7) Connect the signature analyser, in turn, to the points given in Table 9 and check that signatures are obtained. Any output latch connected to the DB0 - DB7 lines may be removed without affecting the correct bus signatures. Input devices however, must not be removed.

Table 9: Routine SA3C Signature

SIGNAL	SIGNATURE	TEST POINT (IC PIN No.)								
		ML2	ML6	ML12	ML13	ML15	ML16	ML17	ML18	ML19
ROW 7	82CP	-	-	-	2	-	-	-	-	-
ROW 6	82CP	-	-	-	4	-	-	-	-	-
ROW 5	82CP	-	-	-	6	-	-	-	-	-
ROW 4	82CP	-	-	-	10	-	-	-	-	-
ROW 3	82CP	-	-	2	-	-	-	-	-	-
ROW 2	82CP	-	-	4	-	-	-	-	-	-
ROW 1	82CP	-	-	6	-	-	-	-	-	-
ROW 0	82CP	-	-	10	-	-	-	-	-	-
TP12	4497	-	-	1	1	-	-	-	-	-
TP25	CFHH	1,15	1	15	-	-	-	-	-	
TP24	64U4	-	5	-	15	1,15	-	-	-	
TP23	CFU2	-	4	-	-	-	-	-	-	
TR1 COL	3P4F	-	-	-	-	-	2,7	2,7	2,7	
EXT.PTT	82CP	-	-	-	-	-	-	-	-	1,2
EXT.MUTE	82CP	-	-	-	-	-	-	-	-	6,7

Table 9 (Cont'd)

SIGNAL	SIGNA-TURE	TEST POINT (IC PIN No.)								
		ML2	ML6	ML12	ML13	ML15	ML16	ML17	ML18	ML19
$\overline{\text{EXT.PTT}}$	0000	-	-	-	-	12	-	-	-	-
$\overline{\text{EXT.MUTE}}$	0000	-	-	-	-	14	-	-	-	5
RF SW	82CP	-	-	14	-	-	-	-	-	-
LINE SW	82CP	-	-	12	-	-	-	-	-	-
VOX SW	82CP	-	-	-	-	2	-	-	-	-
TX SW	82CP	-	-	-	-	4	-	-	-	-
LSB AGC	82CP	-	-	-	12	-	-	-	-	-
USB AGC	82CP	-	-	-	14	-	-	-	-	-
DB0	5AC8	-	-	9	-	11	-	-	-	-
DB1	5AC8	-	-	7	-	13	-	-	-	-
DB2	CFU2	11	-	5	-	-	-	-	-	-
DB3	8291	13	-	3	-	-	-	-	-	-
DB4	64HC	3	-	-	9	-	-	-	-	-
DB5	64HC	5	-	-	7	-	-	-	-	-
DB6	CFHH	7	-	-	11,5	-	-	-	-	-
DB7	CFHH	9	-	-	13,3	-	-	-	-	-
VOX	0000	-	-	-	-	6	-	-	-	-

Routine SA3D - Display Board

45. (1) Set the MA1723 POWER switch to OFF.

(2) Lower the MA1723 front panel assembly (as detailed in para. 41(3) and 41(4).

(3) Remove the nine screws, each with a crinkle washer, securing the front panel interface board to the front panel assembly.

(4) Disconnect the coaxial socket from PL39 on the front panel interface board.

(5) Raise the front panel interface board to reveal the front panel display board.

(6) Place a sheet of card or other insulating material between the underside of the raised front panel interface board and the exposed stand-off pillars securing the front panel display board.

(7) Connect the signature analyser leads as follows:

START)	ML5 pin 12, Front	
STOP)	Panel interface board	
CLOCK	TP1	) Processor
GROUND	Lower end of R2)	board

(8) Ensure that:

(a) Switches SB and SF on the processor board are both set to the closed (UP) position.

(b) Switches SA, SC, SD and SE on the processor board are set to the open (down) position.

(c) The AGC switches SA and SB on the modulation board are both set to the open (OFF) position.

(d) The LINE/SET/RF switch is set to the SET position.

(e) The VOX/PTT/TX switch is set to the PTT position.

(9) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	OUT (positive edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(10) Set the MA1723 POWER switch to ON.

(11) Connect the signature analyser probe, in turn, to the following points on the front panel display board and check that correct signatures are obtained.

+5V	- Positive end of C1	-	8U93
0V	- Negative end of C1	-	0000

(12) Connect the signature analyser probe, in turn, to the points given in tables 10, 11 and 12, and check that correct signatures are obtained. Any display driver integrated circuit may be removed without affecting the correct signatures.

(13) Set the front panel POWER switch to OFF.

(14) Re-assemble the front panel interface board to the front panel assembly.

Table 10: Routine SA3D Signatures 1

SIGNAL	SIGNATURE	TEST POINT (IC PIN No.)							
		ML13 to ML21	ML12	ML9	ML8	ML25	ML6	ML4	ML26
DB0	UUOF	5	9	5	5	9	9	9	3
DB1	HP49	3	11	3	3	11	11	11	4
DB2	5319	2	13	2	2	13	13	13	6
DB3	9UPP	4	15	4	4	15	15	15	1

Table 11: Routine SA3D Signatures 2

SIGNAL	SIGNATURE	TEST POINT (IC PIN No.)					
		ML2	ML3	ML5	ML24	ML7	ML26
DB4	C646	9	9	9	-	9	13
DB5	HA85	11	11	11	-	11	14
DB6	6U62	13	13	13	13	13	-
DB7	UOUA	15	15	15	15	15	-

Table 12: Routine SA3D Signatures 3

SIGNAL	SIGNATURE	ML10	SIGNAL	SIGNATURE	ML10
S0	5290	11	S11	F8P8	19
S1	4095	9	S12	381F	14
S2	C304	10	S13	3F33	13
S3	930C	8	S14	8363	16
S4	53H9	7	S15	013C	15
S5	9725	6	N0	93H2	2
S6	H599	5	N1	9H03	3
S7	485H	4	N2	U891	21
S8	7CH4	18	N3	24H7	22
S9	H097	17	STROBE	8U40	23
S10	8P3H	20			

Routine SA3E - Modulation Board

46. (1) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	OUT (positive edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(2) Set the MA1723 POWER switch to OFF.

(3) Connect the signature analyser leads as follows:

START)	ML5 pin 12, Front	
STOP)	panel interface board	
CLOCK	TP1	) Processor
GROUND	Lower end of R2)	board

(4) Ensure that:

(a) Switches SB and SF on the processor board are both set to the closed (UP) position.

(b) Switches SA, SC, SD and SE on the processor board are set to the open (down) position.

(c) The AGC switches SA and SB on the modulation board are both set to the open (OFF) position i.e. towards the board edge.

(d) The LINE/SET/RF switch is set to the SET position.

(e) The VOX/PTT/TX switch is set to the PTT position.

(5) Set the MA1723 POWER switch to ON.

(6) Connect the signature analyser probe, in turn, to the following points on the modulation boad and check that correct signatures are obtained.

+5V	- ML26 pin 1	-	8U93
0V	- ML26 pin 8	-	0000

(7) Connect the signature analyser probe, in turn, to the points given in Tables 13, 14, 15 and 16, and check that correct signatures are obtained. As an aid to locating a device which is causing incorrect signatures on the modulation board data bus D0 to D7, any of the latches ML19, ML20, ML21, ML22 or ML29 may be removed without affecting the correct bus signatures.

Table 13: Routine SA3E Signatures 1

SIGNAL	SIGNATURE	TEST POINT (IC PIN No.)						
		ML19	ML20	ML21	ML22	ML27	ML28	ML29
DB0	UUOF	-	-	-	-	-	10	-
DB1	HP49	-	-	-	-	-	3	-
DB2	5319	-	-	-	-	-	6	-
DB3	9UPP	-	-	-	-	-	14	-
DB4	C646	-	-	-	-	6	-	-
DB5	HA85	-	-	-	-	3	-	-
DB6	6U62	-	-	-	-	10	-	-
DB7	UOUA	-	-	-	-	14	-	-
D0	UUOF	-	-	4	4	-	-	-
D1	HP49	-	-	7	7	-	-	-
D2	5319	-	-	13	13	-	-	-
D3	9UPP	-	-	14	14	-	-	-
D4	C646	14	4	-	-	-	-	4
D5	HA85	13	7	-	-	-	-	7
D6	6U62	7	13	-	-	-	-	13
D7	UOUA	4	14	-	-	-	-	14

Table 14: Routine SA3E Signatures 2

SIGNAL	SIGNATURE	TEST POINT (IC PIN No.)					
		ML12	ML16	ML22	ML29	ML31	ML32
B0	0A77	-	-	2	-	-	-
B2	2962	-	-	11	-	-	2
B3	P713	-	-	1	-	-	6,7
B4	0AH4	-	-	-	2	5	-
B5	89H0	12	-	-	10	-	-
B6	8HU7	6	-	-	11	-	-
B7	6127	-	12,6	-	1	-	-
CARRIER	2336	13,5	-	-	-	-	3

Table 15: Routine SA3E Signatures 3

SIGNAL	SIGNATURE	TEST POINT (IC PIN No.)						
		ML2	ML5	ML7	ML16	ML20	ML21	ML30
LSB+AGC	6668	-	-	6	-	10	-	9
LSB-AGC	644U	-	-	12	-	2	-	8
USB+AGC	892C	5	-	-	-	-	1	13
USB-AGC	3AF0	13	-	-	-	-	11	12
A	09UP	-	10	-	-	-	2	-
B	8U3P	-	9	-	-	-	10	-
2A6	C953	6	-	13	13	11	-	-
2A7	C98H	12	-	5	5	1	-	-

Table 16: Routine SA3E Signatures 4

SIGNAL	SIGNATURE	TEST POINT (IC PIN No.)						
		ML19	ML20	ML21	ML22	ML24	ML26	ML29
OP2A	F55C	-	-	-	-	-	14	-
OP2B	4716	-	-	-	-	-	3	-
OP2C	32C1	-	-	-	-	-	6	-
OP2A	F55C	-	5	5	-	-	13	-
OP2B	4716	-	-	-	5	-	4	5
OP2C	32C1	5	-	-	-	-	5	-
C	F9UU	2	-	-	-	9	-	-
B	UF48	10	-	-	-	10	-	-
A	U344	11	-	-	-	11	-	-

(8) Set the MA1723 POWER switch to OFF.

(9) Replace the front panel assembly.

Routine SA3F - Synthesizer Board Input Data

47. (1) Stand the unit so that it rests on the left-hand side member.

(2) Remove the push-fit screening cover from the synthesizer board compartment.

(3) Remove the six-side screening plate from the synthesizer board, secured with four captive screws.

(4) Follow the procedures given in paras. 46(1) to 46(4).

(5) Set the MA1723 POWER switch to ON.

(6) Connect the signature analyser probe, in turn, to the following points on the synthesizer board, and check that correct signatures are obtained.

+5V - ML12 pin 39 - 8U93
0V - ML12 pin 24 - 0000

(7) Connect the signature analyser probe, in turn, to the points given in table 17 and check that correct signatures are obtained.

Table 17: Routine SA3F Signatures

SIGNAL	SIGNA-TURE	ML12 PIN
DB0	UU0F	22
DB1	HP49	21
DB2	5319	20
DB3	9UPP	19
DB4	C646	18
OP29	P03H	17

(8) Set the MA1723 POWER switch to OFF.

(9) Disconnect all test equipment and replace all removed items (except the screening cover and plate from the synthesizer board if proceeding with self-test routine 21 - para. 48).

(10) Set switches SA to SF on the processor board to the open (down) position.

(11) Set the AGC switches SA and SB on the modulation board as required (the OFF position is towards the board edge).

Self-Test Routine 21

48. Self-test routine number 21 is a signature analysis routine for the synthesizer board. Due to the waveshape of the signal at TP8 on the synthesizer board, one of four possible sets of valid signatures may be obtained at the points given, and hence four sets of signatures are listed (in table 18). The procedure is as follows:

49. (1) Set the MA1723 POWER switch to OFF.

(2) Stand the unit so that it rests on the left-hand side member.

(3) Remove the push-fit screening cover from the synthesizer board compartment.

(4) Remove the six-sided screening plate from the synthesizer board, secured with four captive screws.

(5) Ensure that switches SA to SF on the processor board are all set to the open (down) position.

(6) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	IN (negative edge)
CLOCK pushbutton	IN (negative edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(7) Connect the signature analyser leads to the following test points on the synthesizer board:

START	TP8
STOP	TP8
CLOCK	TP6
GROUND	TP3

(8) Set the MA1723 POWER switch to ON.

(9) Press and hold the REM pushbutton, press and release the numeral 2 pushbutton followed by the numeral 1 pushbutton, and then release the REM pushbutton.

(10) Check that the MA1723 front panel displays are blanked apart from a flashing test number 21.

(11) Press and release the ENTER pushbutton to start the routine.

(12) Connect the signature analyser probe, in turn, to the following points on the synthesizer board and check that correct signatures are obtained.

+5V - ML12 pin 39 - 21F5
0V - ML12 pin 24 - 0000

(13) Connect the signature analyser probe, in turn, to the points given in table 18 and check that correct signatures (either A, B, C or D) are obtained.

(14) Switch off and disconnect all test equipment.

(15) Replace all removed items.

Table 18: Self-test Routine 21 Signatures

SIGNAL	SIGNATURE				TEST POINT (IC PIN No.)			
	A	B	C	D	ML12	ML18	ML11	ML19
DIV 1	51P4	825H	6U49	94AU	13	3	-	-
DIV 2	2H7P	9081	29AA	A246	12	4	-	-
DIV 3	0FCC	C144	086U	8383	11	5	-	-
DIV 4	0000	0000	0000	0000	10	6	-	-
DIV 5	21F5	21F5	21F5	21F5	9	-	3	-
DIV 6	21F5	21F5	21F5	21F5	8	-	4	-
DIV 7	21F5	21F5	21F5	21F5	7	-	5	-
DIV 8	0000	0000	0000	0000	6	-	6	-
DAC 1	028A	8P55	4PP9	4F45	33	-	-	5
DAC 2	9845	C919	9A77	664A	32	-	-	6
DAC 3	U2HU	A47P	46FC	C9U3	31	-	-	7
DAC 4	3508	A038	82A7	F56A	30	-	-	8
DAC 5	9F0H	3P0F	1A29	0A7H	29	-	-	9
DAC 6	0UA8	62C0	15A3	4717	28	-	-	10
DAC 7	6600	6478	FU81	8044	27	-	-	11
DAC 8	4F9A	6H5U	825C	A39P	26	-	-	12

Racal Communications Limited

Amendment to

MA 1723 HF Drive Unit

CR 74089

Chapter 7
Components 3

C29 Change to 10n ±10% 50V 940315

Chapter 8
Components 5

C53, C55, & C60 Change to 10n ±10% 50V 940315

Chapter 9
Components 2

C3, C6, & C17 Change to 10n ±10% 50V 940315

Chapter 10
Components 7 & 8
C53, C54, C55, C56, C67, C85, C86 & C102

Change to 10n ±10% 50V 940315